

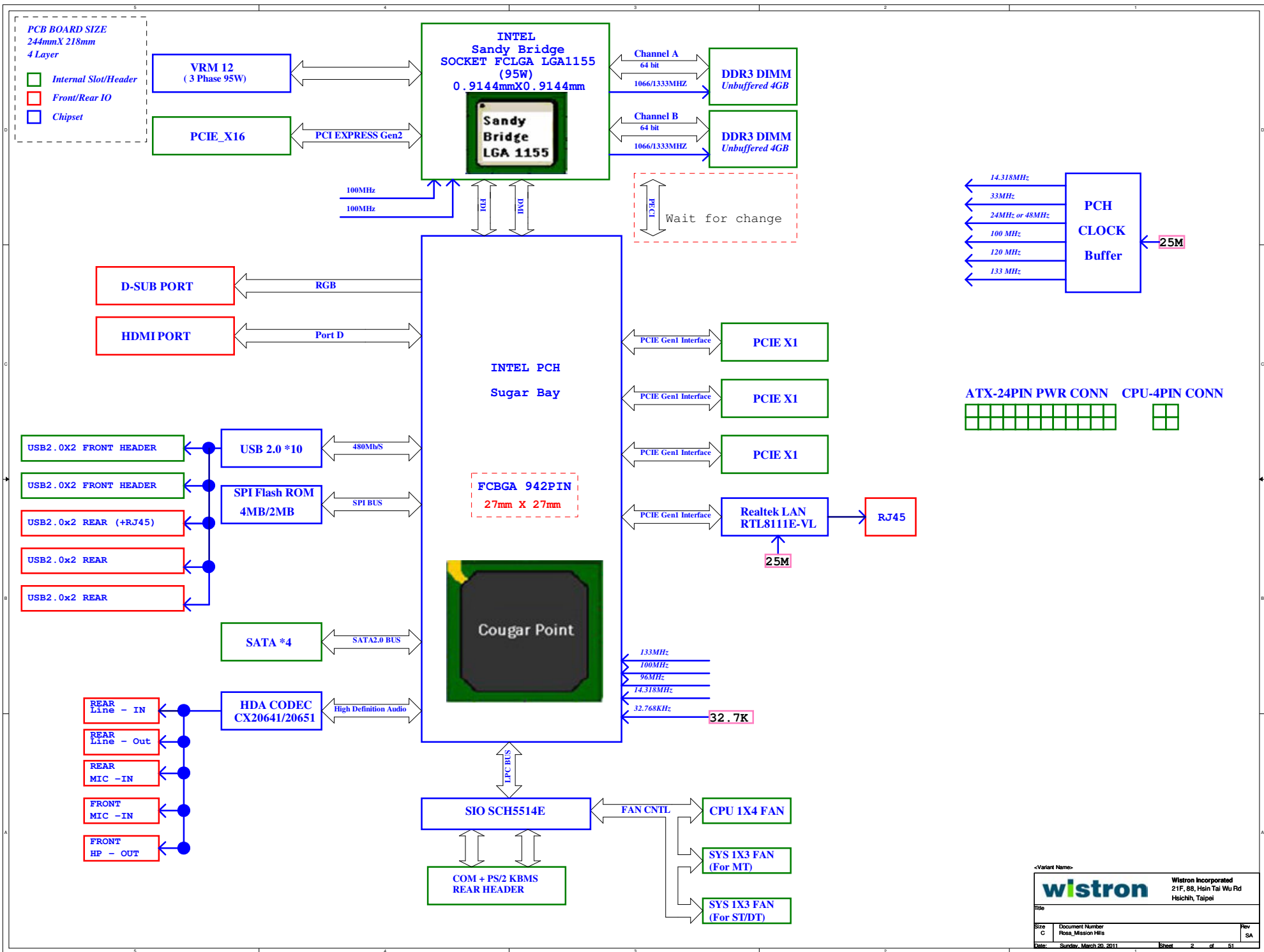
Model: Mission Hills/Sawgrass  
 PCB Ver: A00  
 PCB Number: 10097-1  
 SCH Ver: 06  
 PCBA:

PAGE	TITLE	Quantity
01	Cover Page	
02	BLOCK DIAGRAM	
03	Power Delivery	
04	POWER GOOD AND RESET DIAGRAM	
05	CLOCKS DIAGRAM	
06	Power Sequence	
07	POWER Map	
08	GPIO	
09	CLOCK GEN - CK505	
10	CPU LGA 1155_1	
11	CPU LGA 1155_2	
12	CPU LGA 1155_3	
13	CPU LGA 1155_4	
14	XDP/80 PORT HEADER	
15	DDR3 CHA DIMM 0	
16	TBD	
17	DDR3 CHB DIMM 0	
18	TBD	
19	PCH Cougar AUDIO/GPIO/SPI	
20	PCH Cougar CLK/FDI/ONFI	
21	PCH Cougar SATA/FAN/DP	
22	PCH Cougar PCI/PCIE/DMI/USB	
23	PCH Cougar GND/STRAPS	
24	PCH Cougar POWER	
25	SATA Port	
26	PCIEX16 CONNECTOR	
27	VGA Port	
28	HDMI Port	
29	TBD	
30	FRONT USB	
31	USB+RJ45 / REAR USB	
32	Gb LAN RTL8151ED	
33	AUDIO CX20641/CX20651	
34	AUDIO CODEC JACKS	
35	DSW	
36	SIO SCH5514E	
37	KeyBoard and MouSe	
38	Serial & Parallel port	
39	FAN CIRCUITS/HOLE	
40	TBD	
41	PCIEX1 CONNECTOR	
42	TBD	
43	TBD	
44	TBD	
45	PWR/FNT PNL	
46	DUAL POWER	
47	DDR POWER	
48	SYSTEM POWER	
49	CPU VTT & CPU SA	
50	CPU VRD 12-1 & CPU AXG	
51	CPU_VRD 12-2	

PCB BOARD SIZE  
 4 Layers  
 244mmX 218mm

BOM Configuration  
 Unmount: (R)  
 Unmount after MP (X)

SB BUILD  
 Sugar Bay :  
 LGA1155 : Sandy Brighe  
 Chipset : Cougar Point H61  
 LAN : Gb LAN RTL8151ED



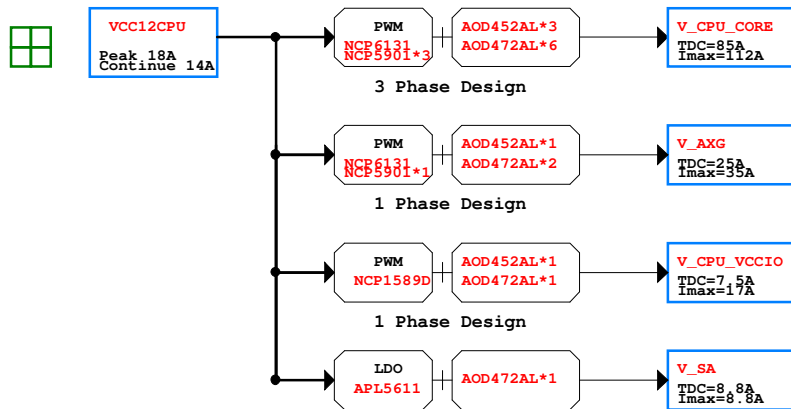
<Variant Name>

**wistron**

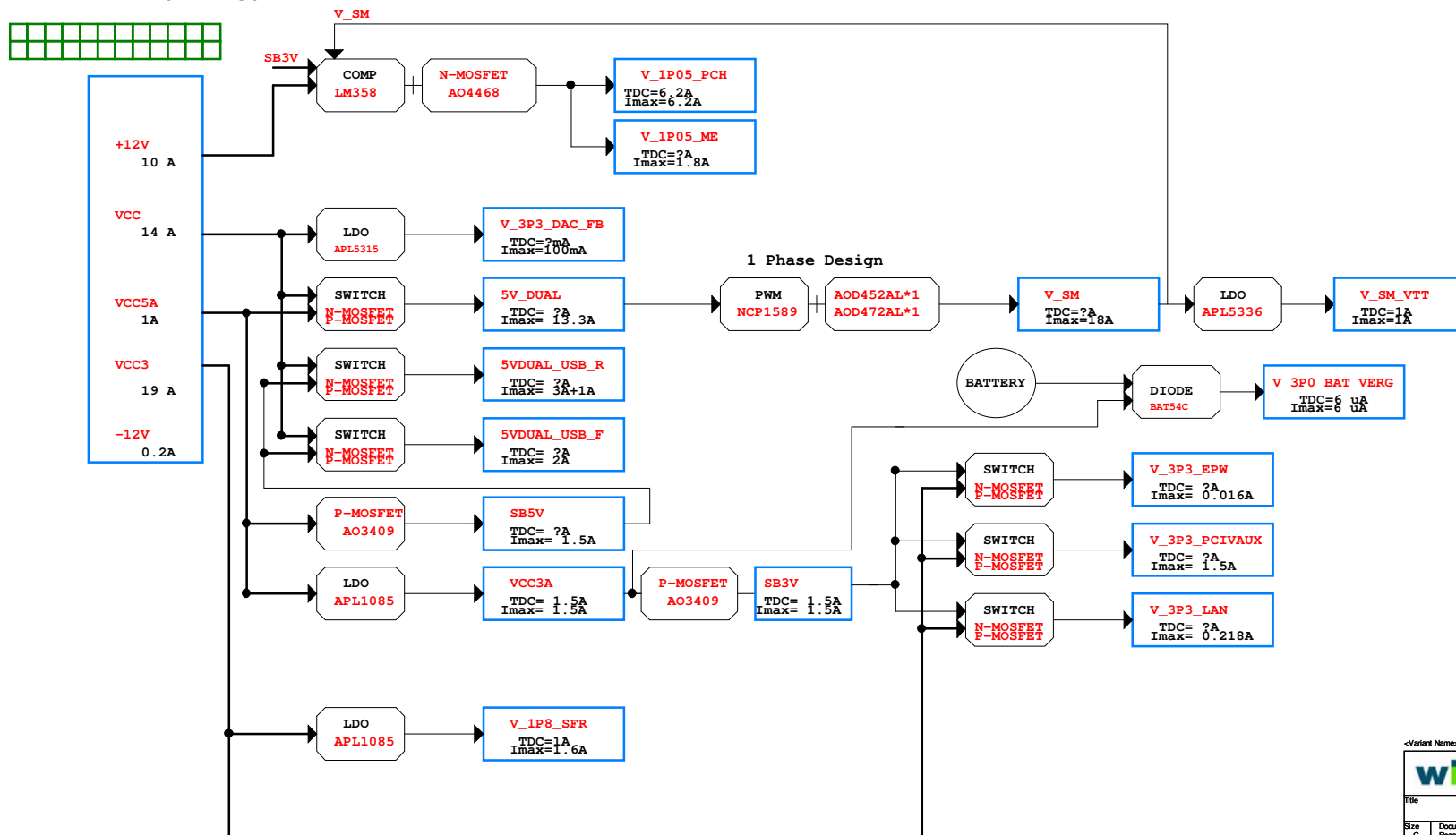
Wistron Incorporated  
21F, 88, Hei Tai Wu Rd  
Hsichih, Taipei

Title		
Size	Document Number	Rev
C	Pass_Mission Hills	SA
Date:	Sunday, March 20, 2011	Sheet 2 of 51

## CPU 2X2 POWER CONN



## ATX 2X12 POWER CONN



<Variant Name>

**wistron**

Wistron Incorporated  
21F, 88, Hei Tai Wu Rd  
Hsichih, Taipei

Title

Size

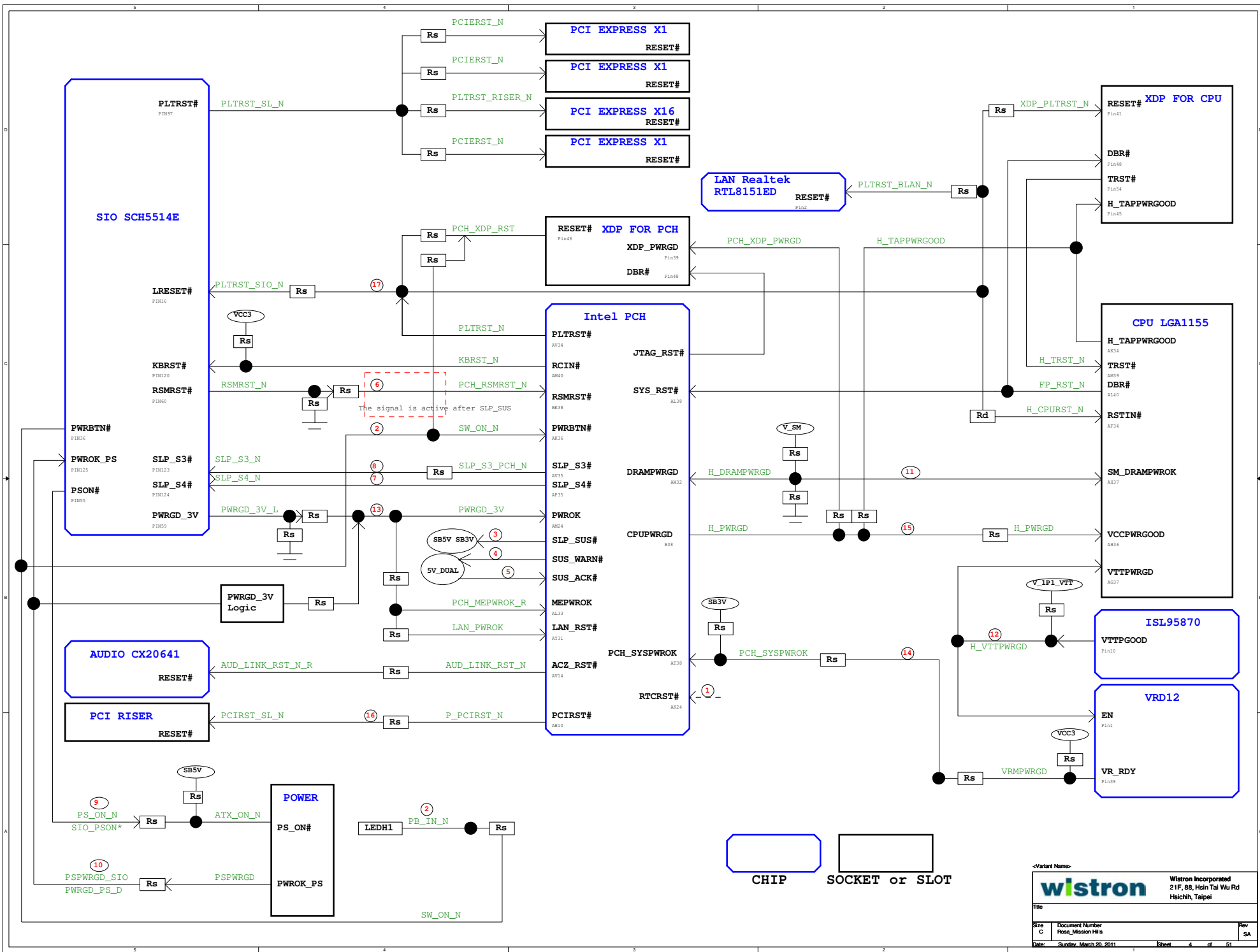
Document Number  
Pesa\_Mission Hills

Rev

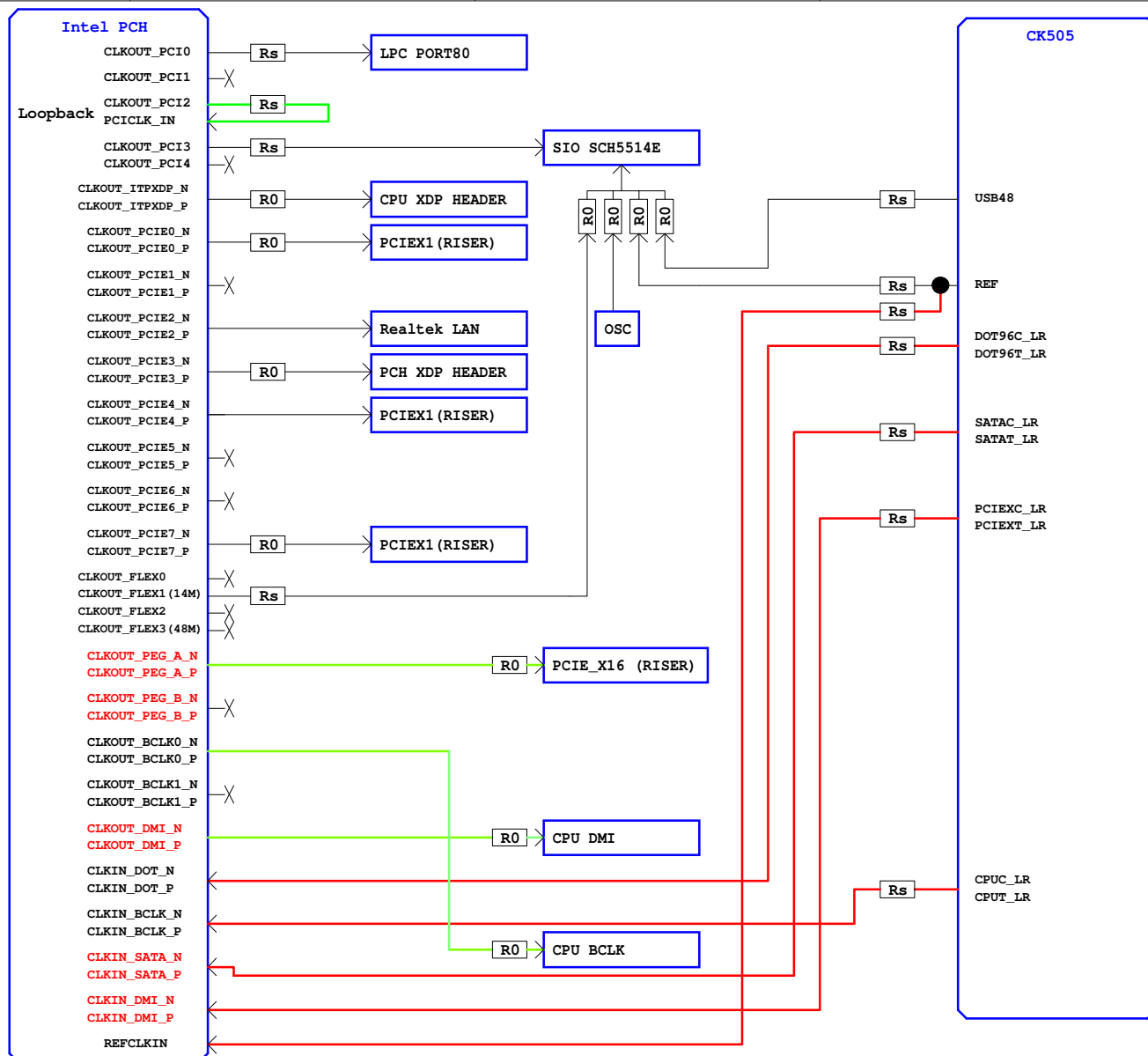
SA

Date: Sunday, March 20, 2011

Sheet 3 of 51



CHIP SOCKET or SLOT



BTM: Buffer Through Mode  
Need CK505 to provide 4 clock to PCH

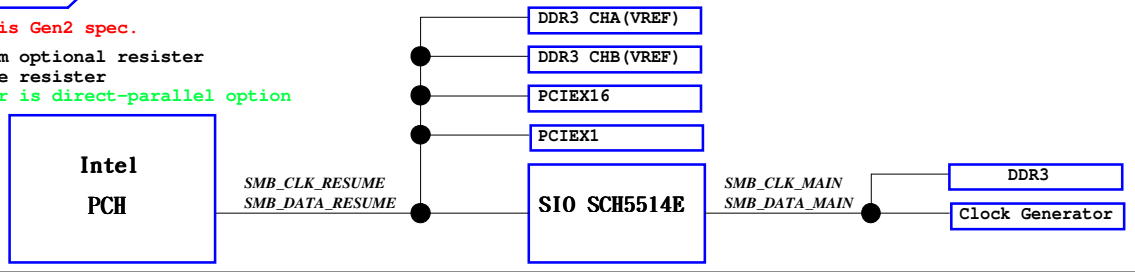
FCIM: Full Clock Intergration Mode  
Remove CK505

Note: Red Color is Gen2 spec.

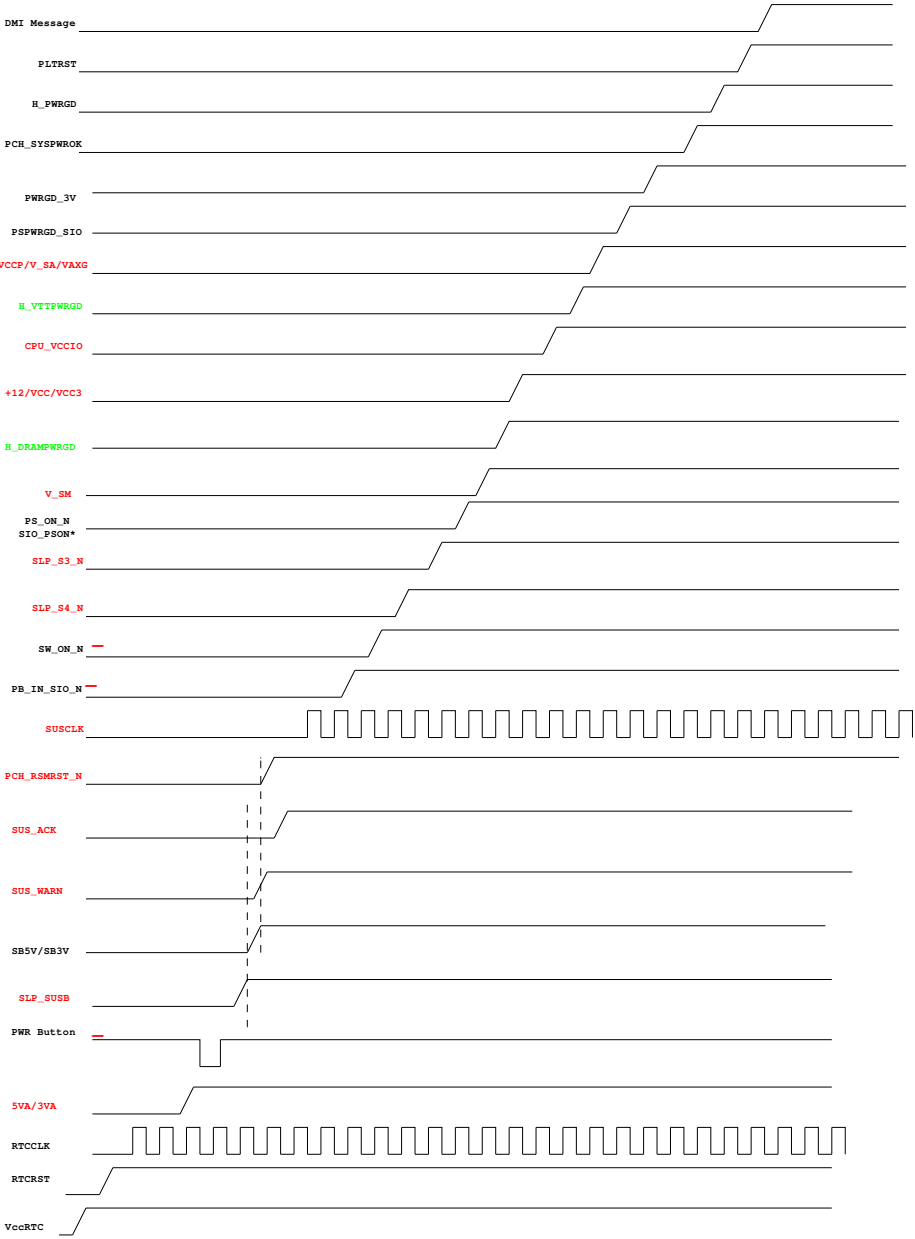
Note: R0 is 0 ohm optional resistor

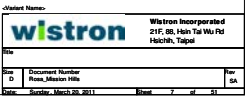
Note: Rs is serie resistor

Note: Green Color is direct-parallel option



POWER ON SEQUENCE





## PCH (H61)

PIN NAME	Pin#	POWER WELL	USAGE	BIOS Post Value	Default Type	Notes
GPIO0	AW52	MAIN	PCD_REG_N	GPI (No Use)	GPI	10K P/U to VCC3 MAIN
GPIO1	BR19	MAIN	HDMI_DETECT	GPI (Low: NO HDMI, High: HDMI detect )	GPI	1 P/U 20K
GPIO2	BN8	MAIN	P_INT_E_N	GPI (No Use)	GPI	Unused,8.2K P/U to VCC3 MAIN
GPIO3	AV9	MAIN	P_INTF_N	GPI (No Use)	GPI	Unused,8.2K P/U to VCC3 MAIN
GPIO4	BT15	MAIN	P_INTG_N	GPI (No Use)	GPI	Unused,8.2K P/U to VCC3 MAIN
GPIO5	BR4	MAIN	P_INTH_N	GPI (No Use)	GPI	Unused,8.2K P/U to VCC3 MAIN
GPIO6	BA22	MAIN	TACH2	GPI (No Use)	GPI	Unused,10K P/U to VCC3 MAIN,1 P/U 20K
GPIO7	BR16	MAIN	TACH3	GPI (No Use)	GPI	Unused,10K P/U to VCC3 MAIN,1 P/U 20K
GPIO8	BP51	RESUME	IO_SMI_N	GPI (IO_SMI_N)	GPO	10K P/U to SB3V
GPIO9	BJ41	RESUME	USB_OC5_R_N	NATIVE	Native	USB OVER CURRENT
GPIO10	BT45	RESUME	USB_OC6_R_N	NATIVE	Native	10K P/U to SB3V
GPIO11	BM49	RESUME	LPC_PME_N	GPI (LPC_PME_N)	Native	LPC_PME_N,10K P/U to SB3V
GPIO12	BK50	RESUME	PCH_HEATSINK_DETECT (Reserved)	GPI (Low: PCH Heatsink detected, High: No PCH Heatsink)	Native	10K P/U to SB3V
GPIO13	BA25	RESUME	PWR_CLEAR	GPI (High: Normal, Low: Clear Password)	GPI	10K P/U to SB3V, with a Jumper to GND
GPIO14	BM45	RESUME	USB_OC7_R_N	NATIVE	Native	10K P/U to SB3V
GPIO15	BM55	RESUME	TLS_EN	GPO (Unused)	GPO	1 P/D 20K (Strapping)
GPIO16	AU56	MAIN	FB_USB2_DET	GPI (Low: Front USB detected, High: No Front USB)	GPI	10K P/U to VCC3 MAIN
GPIO17	BT17	MAIN	TACH0	GPI (No Use)	GPI	Unused,10K P/U to VCC3 MAIN
GPIO19	AV52	MAIN	SATAGP	GPI (No Use)	GPI	Unused,10K P/U to VCC3 MAIN (Strapping)
GPIO20	AV43	MAIN	BOARD_ID_0	GPI (No Use)	Native	10K P/U to VCC3 MAIN,10K (R) P/D to GND
GPIO21	BC54	MAIN	FB_USB1_DET	GPI (Low: Card Reader detected, High: No Card Reader)	GPI	FB_USB1_DET,10K P/U to VCC3 MAIN
GPIO22	BA53	MAIN	BIOS_RCY_GP22	GPI (No Use)	GPI	BIOS_RCY_GP22,10K P/U to VCC3 MAIN
GPIO23	BA20	MAIN	LPC_DRQ1_N	GPI (Not required for test)	Native	Unused,1 P/U 20K
GPIO24	BP53	RESUME	H_SKT0CC_R_N	GPI (Low: CPU detected, Floating: No CPU)	GPO	H_SKT0CC_R_N,1K(R) P/U to +3P3V, AUX,10K(R) P/D to GND
GPIO27	BJ43	ep Sleep Power W	PCH_GP27_PU	GPI (Unused)	GPI	10K P/U to V_3P3_A
GPIO28	BJ55	RESUME	PCH_GP28_PU	GPO (Unused)	GPO	10K(R) P/U to V_3P3_A
GPIO29	BM49	RESUME	SLP_LAN_N	GPO (S0/S5 Low, S3 High) S5 Low to turn off LAN power in S5	Native	LAN Enable/Disable
GPIO30	BU46	RESUME	SUS_WARNB	NATIVE	GPI	Function Pin
GPIO31	BG43	ep Sleep Power W	PCH_GP31_PU	GPI (Unused)	GPI	10K P/U to V_3P3_A
GPIO32	BC56	MAIN	EXT_MUTEW	GPO (50 High, S3/S5 Low) S3/S5 Low to mute external speaker	GPO	External Mute
GPIO33	BC25	MAIN	SOP_ENABLE_GP33	Unused (GPI)	GPO	10K P/U to VCC3 MAIN,1 P/D 20K
GPIO34	BL56	MAIN	SPK_DETECT	GPI (Low: Speaker detected, High: No Speaker)	GPI	SPK_DETECT,10K P/U to VCC3 MAIN
GPIO35	BJ57	MAIN	SPK_MUTEW	GPO (50 High, S3/S5 Low) S3/S5 Low to mute external speaker	GPO	SPK_MUTEW,10K P/U to VCC3 MAIN
GPIO36	BB55	MAIN	SATA2GP	GPI (Unused)	GPI	Unused,10K(R) P/U to VCC3 MAIN
GPIO37	BB53	MAIN	SATA3GP	GPI (Unused)	GPI	Unused,10K P/U to VCC3 MAIN
GPIO38	BE54	MAIN	CHASSIS_ID_0	GPI (Pis refer to <a href="#">Table 3</a> table)	GPI	CHASSIS_ID_0,10K P/U to VCC3 MAIN
GPIO39	BF55	MAIN	CHASSIS_ID_1	GPI (Pis refer to <a href="#">Table 3</a> table)	GPI	CHASSIS_ID_1,10K P/U to VCC3 MAIN
GPIO40	BD41	RESUME	USB_OC1_R_N	NATIVE (OC1W)	Native	USB OVER CURRENT
GPIO41	BG41	RESUME	USB_OC2_R_N	NATIVE (OC2W)	Native	USB OVER CURRENT
GPIO42	BK43	RESUME	USB_OC3_R_N	NATIVE (Unused)	Native	10K P/U to SB3V
GPIO43	BF43	RESUME	USB_OC4_R_N	NATIVE (OC4W)	Native	USB OVER CURRENT
GPIO44	BL54	RESUME	LAN_EN	GPI (High: LAN enable, Low: LAN disabled) S0/S5 High: SB3V/S3 Low: SB3V/S5 High	Native	10K P/U to SB3V,10K(R) P/D to GND
GPIO45	AV44	RESUME	1_WATT_CTRL_1	GPO (S0/S5 High, S3 Low) S5 High to turn off PCIAUX 3.3V	Native	1_WATT_CTRL_1,10K P/U to SB3V,10K(R) P/D to GND
GPIO46	BP55	RESUME	INTRU_DET	GPI (Low: Intruder Cable detected, High: No Cable)	Native	INTRU_DET,10K P/U to SB3V,1K(R) P/D to GND
GPIO48	AW53	MAIN	MTST_ID	GPI (High: Slim Tower, Low: Mini Tower) (Pis refer to <a href="#">Table 3</a> table)	GPI	MTST_ID,10K P/U to VCC3 MAIN
GPIO49	BA56	MAIN	VGA_DET	GPI (High: VGA detected, Low: No VGA)	GPI	VGA_DET,10K P/U to VCC3 MAIN
GPIO50	BT5	MAIN	P_REQ_N1	NATIVE (Unused)	Native	Function Pin,8.2K P/U to VCC3 MAIN
GPIO51	AV8	MAIN	P_REQ_N1	NATIVE (Unused)	Native	Strap Pin,1K(R) P/D GND,1 P/U 20K
GPIO52	BR8	MAIN	P_REQ_N2	NATIVE (Unused)	Native	Function Pin,8.2K P/U to VCC3 MAIN
GPIO53	BU12	MAIN	P_REQ_N2	NATIVE (Unused)	Native	Strap Pin,1K(R) P/D GND,1 P/U 20K
GPIO54	AV11	MAIN	P_REQ_N3	NATIVE (Unused)	Native	Function Pin,8.2K P/U to VCC3 MAIN
GPIO55	BE2	MAIN	P_GNT_N3	NATIVE (Unused)	Native	Strap Pin,1K(R) P/D GND,1 P/U 20K
GPIO57	BT53	RESUME	ME_CNTL	GPI (High: BIOS OK, Low: BIOS Error)	GPI	Unused,10K(R) P/U to SB3V,47K P/D GND
GPIO58	BJ46	RESUME	SMLCLK_PCH	NATIVE (Unused)	Native	SMLCLK_PCH,10K P/U to SB3V
GPIO59	BM43	RESUME	USB_OC0_R_N	NATIVE	Native	USB OVER CURRENT
GPIO60	BU49	RESUME	SMLALERT_PCH	NATIVE (Unused)	Native	SMLALERT_PCH,2.2K P/U to SB3V
GPIO61	BM54	RESUME	SUS_STAT_N	NATIVE	Native	W_DISABLE_N,10K P/U (R) to SB3V
GPIO62	BA47	RESUME	SUSCLK	NATIVE	Native	Unused, TP
GPIO63	BT50	RESUME	SLP_S5_N	NATIVE	Native	Unused, TP
GPIO64	AH9	MAIN	Test point (CLKOUTFLEX0)	GPO (Unused)	Native	Unused,1 P/D 20K
GPIO65	BA5	MAIN	CK_14M_FLEX	NATIVE (14.318MHz CLK)	Native	14.318MHz CLK for SIO1 P/D 20K
GPIO66	AW5	MAIN	Test point (CLKOUTFLEX2)	GPO (Unused)	Native	Unused,1 P/D 20K
GPIO67	BA2	MAIN	BOARD_ID_1	GPI (Reserved, Board ID 1)	Native	P/D 20K
GPIO68	BU16	MAIN	FP_DETECT (Palm Beach MT/DT Only)	GPI (Low: PWR cable detected, High: No PWR cable)	TBD	10K P/U to VCC3 MAIN
GPIO69	BM18	MAIN	TACH5	Unused	TBD	Unused,10K P/U to VCC3 MAIN
GPIO70	BN17	MAIN	SERIAL_DETECT	GPI (Low: COM Port/KBMS detected, High: No COM/KBMS)	GPI	SERIAL_DETECT,10K P/U to VCC3 MAIN
GPIO71	BP15	MAIN	FP_AUD_DETECT	GPI (Low: Front Audio detected, High: No Front Audio)	GPI	FP_AUD_DETECT,10K P/U to VCC3 MAIN
GPIO72	AV46	RESUME	USB_PWR_CRL1	GPO (S0/S3 High, S5 Low) If board ID is 11 S3 High to turn on USB 5V, S5 Low to turn off USB 5V GPO (S0/S3 Low, S5 High) If board ID is 00 S0 Low to turn on USB 5V, S5 High to turn off USB 5V	GPO	USB_PWR_CRL1,10K P/U to SB3V
GPIO74	BR46	RESUME	SML1ALERT_PCH	NATIVE (Unused)	Native	SML1ALERT_PCH,10K P/U to SB3V
GPIO75	BR46	RESUME	SMLIDATA_PCH	NATIVE (Unused)	Native	SMLIDATA_PCH,10K P/U to SB3V

## SCH5514E

GPIO#	Mux Function	GPIO Function	BIOS Post Value	BIOS Default value	BIOS output type	Pull up/down
GP8051_1	DDC_DATA_2P5V	DIAG_LED1	GPO	Unused, follow original function	GPIO	Open Drain Pull up to VCC3 on I/O Modul
GP8051_2	DDC_CLK_5V	DIAG_LED2	GPO	Unused, follow original function	GPIO	Open Drain Pull up to VCC3 on I/O Modul
GP8051_3	DDC_DATA_5V	DIAG_LED3	GPO	Unused, follow original function	GPIO	Open Drain Pull up to VCC3 on I/O Modul
GP8051_4	DDC_CLK_2P5V	DIAG_LED4	GPO	Unused, follow original function	GPIO	Open Drain Pull up to VCC3 on I/O Modul
GP8051_5	PWRBT1W	Unused	Native	follow original function	Native	Push Pull PCH Internal PR to V_3P3_A
GP8051_6	R1W	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP8051_7	CTS2W	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP8051_8	DSR2W	SMLIDATA_PCH_SIO	GPO (H)	Unused, set as "GPO" to prevent floating	GPIO	Push Pull
GP8051_9	DCD2W	SMLCLK_PCH_SIO	GPO (H)	Unused, set as "GPO" to prevent floating	GPIO	Push Pull
3P8051_10	DCD1W	Unused	Native	follow original function	Native	Input Pull up to VCC3
3P8051_11	DSR1W	Unused	Native	follow original function	Native	Input Pull up to VCC3
3P8051_12	RXD1	Unused	Native	follow original function	Native	Input Pull up to VCC3
3P8051_14	RXD1	Unused	Native	follow original function	Native	Push Pull Pull up to VCC3
3P8051_16	T1S1W	Unused	Native	follow original function	Native	Input
3P8051_16	DDR1W	Unused	Native	follow original function	Native	Push Pull Pull up to VCC3
3P8051_17	R1W	Unused	Native	follow original function	Native	Input Pull up to VCC3
GP10	SLP_S3W	Unused	Native	follow original function	Native	Push Pull
GP11	SLP_S5W	Unused	Native	follow original function	Native	Push Pull
GP14	HD_LEDW	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP21	P16IO31W	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP22	P12/MRT1W/SCSW	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP23	LATCHED_BF_CUT	Unused	Native	follow original function	Native	Push Pull
GP25	SCLK	Unused	Native	follow original function	Native	Open Drain Pull up to VCC3
GP26	SCLK_1	Unused	Native	follow original function	Native	Open Drain Pull up to SB3V
GP31	SECONDARY_HDW	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP33	PRIMARY_HDW	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP35	SDATLED1	Unused	Native	follow original function	Native	Open Drain Pull up to VCC3
GP36	KBORSTW	Unused	Native	follow original function	Native	Open Drain Pull up to VCC3
GP37	A20GATE	Unused	Native	follow original function	Native	Open Drain Pull up to VCC3
GP40	DRIVEN0	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP41	IO_PMEW	Unused	Native	follow original function	GPIO	Open Drain Pull up to SB3V
GP42	SDAT_1YD_SMIW	Unused	Native	follow original function	Native	Open Drain Pull up to SB3V
GP52	RYD2	SLOT0CC_N	NATIVE	reserve, follow original function	GPIO	Push Pull
GP53	TXD2	COPEN_N	NATIVE	reserve, follow original function	GPIO	Push Pull
GP55	RTCWDORC	CPURST_IN	NATIVE	reserve, follow original function	GPIO	Push Pull
GP57	DDR2W	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP60	YELLOW	Unused	Native	follow Power LED behavior function S0/S1: High S3: Low S4/S5: High boot failure (No Post): Low boot failure (Post) Blinking	Native	Open Drain Pull up to SB3V
GP61	GREEN	Unused	Native	follow Power LED behavior function S0/S1: Low S3: High S4/S5: High boot failure (No Post): High boot failure (Post): High	Native	Open Drain Pull up to SB3V
GP75	DE_RSTDRVW	IO_SMI_N	GPO (IO_SMI)	set as "GPO" for SMI function	Native	Open Drain Pull up to SB3V
GP76	PCI_RST_3YSW	Unused	Native	follow original function	Native	Push Pull
GP77	PCI_RST_SL0T5W	Unused	Native	follow original function	Native	Push Pull
GP80	PS_ONW	Unused	Native	follow original function	Native	Open Drain Pull up to V_3P3_A
GP81	BACKFEED_CUTW	Unused	Native	follow original function	Native	Open Drain Pull up to SB3V
GP82	None	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP83	PWR_G00D_3V	Unused	Native	follow original function	Native	Push Pull
GP84	RSMR5TW	Unused	Native	follow original function	Native	Push Pull

&lt;Variant Name&gt;



Wistron Incorporated  
21F, 88, Hei Tai Wu Rd  
Hsichih, Taipei

Title

Size

C

Document Number  
Pss\_Mission Hills

New

SA

Date:

Sunday, March 20, 2011

Sheet

8

of

51

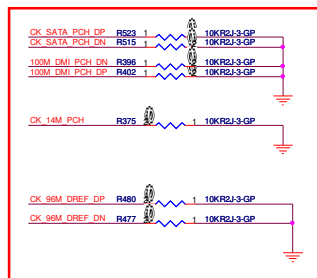


# PCH Buffer CLOCK

22 CK\_96M\_DREF\_DP  
22 CK\_96M\_DREF\_DN  
21 CK\_SATA\_PCH\_DP  
21 CK\_SATA\_PCH\_DN  
22 100M\_DM\_PCH\_DP  
22 100M\_DM\_PCH\_DN

# 14M CLOCK

20 CK\_14M\_PCH



Terminate PCH CLK Inputs

Remove CLK GEN  
Use PCH Internal CLK

<Variant Name>

**wistron**

Wistron Incorporated  
21F, 88, Hei Tai Wu Rd  
Hsichih, Taipei

Title

Size

C

Document Number  
Pesa\_Mission Hills

Rev

SA

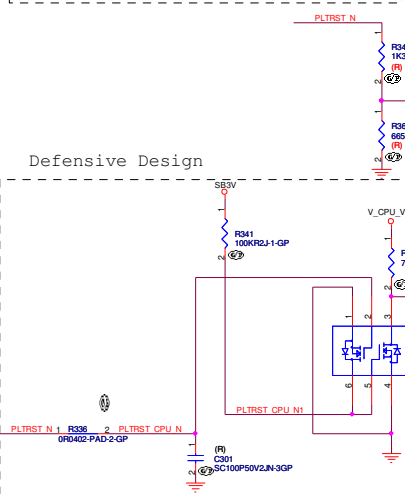
Date: Sunday, March 20, 2011

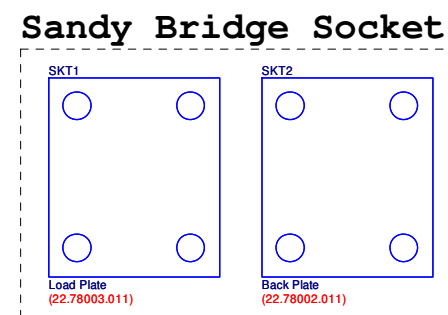
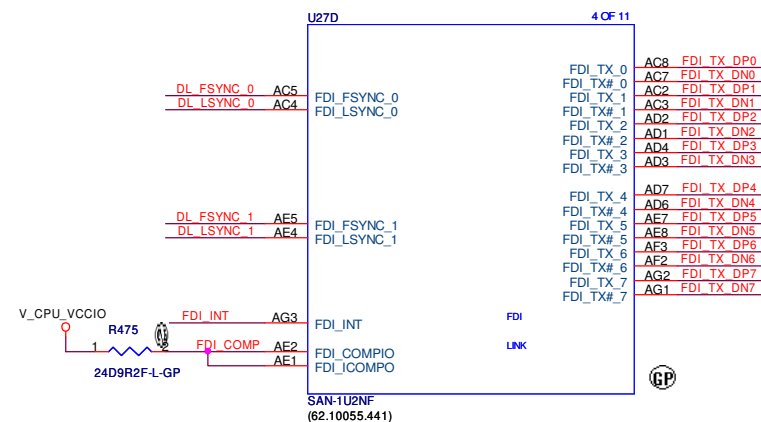
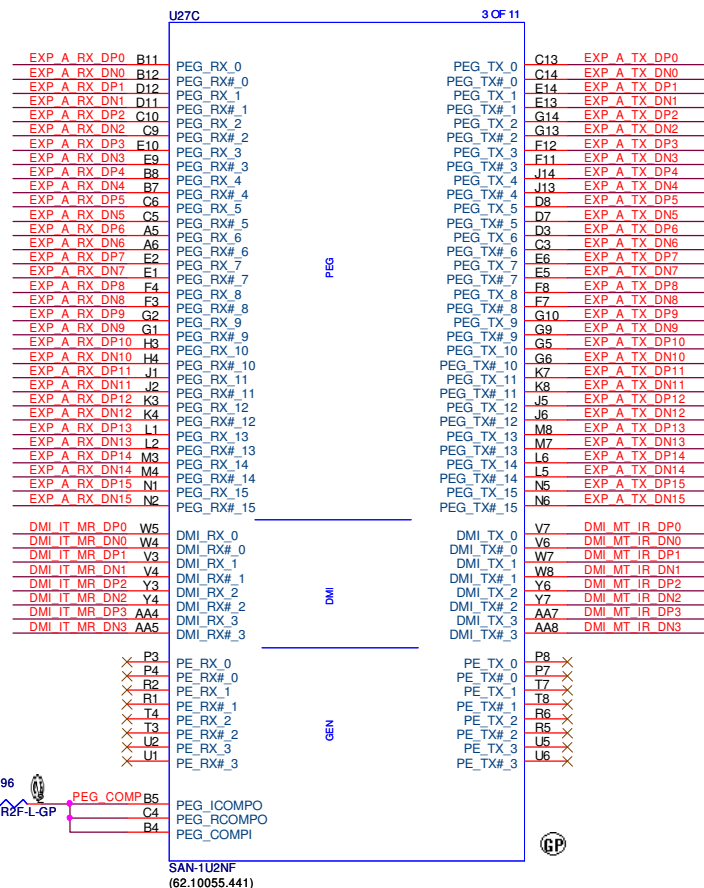
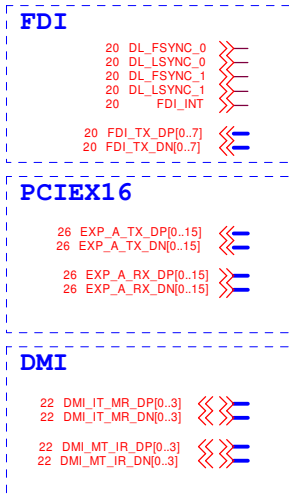
Sheet 9 of 51

- CLOCK**
- 20 CK\_PE\_100M\_MCP\_DP  
20 CK\_PE\_100M\_MCP\_DN
- CPU\_SA**
- 49 VCCA\_VID  
49 VCCA\_SENSE
- CPU\_VTT**
- 49 VCCO\_SEL  
49 VCCO\_SENSE  
49 VSSO\_SENSE
- CPU\_AXG**
- 50 VCCA\_SENSE  
50 VSSA\_SENSE
- CPU\_VCORE**
- 50 VCC\_SENSE  
50 VSS\_SENSE
- ITP**
- 14 H\_TDO  
14 H\_TDI  
14 H\_TCK  
14 H\_TMS  
14 H\_TRST\_N  
14 H\_PROG\_N  
14 H\_PRES\_N
- 14 XDP\_DBRESET\_N  
14 CK\_XDP\_S\_DN  
14 CK\_XDP\_S\_DP
- 14 H\_BPM0  
14 H\_BPM1  
14 H\_BPM2  
14 H\_BPM3  
14 H\_BPM4  
14 H\_BPM5  
14 H\_BPM6  
14 H\_BPM7
- 14.36 H\_CPURST\_N
- OTHER**
- 14,19.36 PLTRST\_N  
14,19 H\_PWRGD  
19 FP\_RST\_DBR\_N
- 19.46 H\_DRAMPWRGD  
21.36 H\_PECI  
36.50 H\_PROCHOT\_N
- 21 H\_THERMTRIP\_N
- 21 H\_PM\_SYNC\_0  
19.36 H\_SKT0CC\_N  
14.36 H\_CPURST\_N
- 23 H\_SNB\_N
- 19.26,32,36.41 SMB\_CLK\_RESUME  
19.26,32,36.41 SMB\_DATA\_RESUME
- 14 TPEV\_SNB\_POUDEBUG\_0

MINIMIZE STUB BETWEEN THESE AND RESISTORS AT SIM PAGE  
PLACE IN CNV AREA

H\_VIDSCK VR R355 1 0P04 PAD-2-GP H\_VIDSCK  
H\_VIDSOUT VR R350 1 0P04 PAD-2-GP H\_VIDSOUT  
H\_VIDALERT N VR R329 1 0P04 PAD-2-GP H\_VIDALERT\_N





## DDR DATA

15 M\_DATA\_A[0..63]  
17 M\_DATA\_B[0..63]  
15 M\_DQS\_A\_DP[0..8]  
16 M\_DQS\_A\_DNP[0..8]  
17 M\_DQS\_B\_DP[0..8]  
17 M\_DQS\_B\_DNP[0..8]

15 M\_DATA\_A\_CB[0..7]  
17 M\_DATA\_B\_CB[0..7]

## DDR CMD/ADD

15 M\_MAA\_A[0..15]  
17 M\_MAA\_B[0..15]  
15 M\_WE\_A\_N  
15 M\_CAS\_A\_N  
15 M\_RAS\_A\_N  
15 M\_SBS\_A0  
15 M\_SBS\_A1  
15 M\_SBS\_A2  
17 M\_WE\_B\_N  
17 M\_CAS\_B\_N  
17 M\_RAS\_B\_N  
17 M\_SBS\_B0  
17 M\_SBS\_B1  
17 M\_SBS\_B2

## DDR CTRL

15 M\_SCS\_A\_N0  
15 M\_SCS\_A\_N1  
15 M\_SCKE\_A0  
15 M\_SCKE\_A1  
15 M\_COT\_A0  
15 M\_COT\_A1

17 M\_SCS\_B\_N0  
17 M\_SCS\_B\_N1  
17 M\_SCKE\_B0  
17 M\_SCKE\_B1  
17 M\_COT\_B0  
17 M\_COT\_B1

## DDR CLOCK

15 CK\_M\_DDR0\_A\_DP  
15 CK\_M\_DDR0\_A\_DN  
15 CK\_M\_DDR1\_A\_DP  
15 CK\_M\_DDR1\_A\_DN

17 CK\_M\_DDR0\_B\_DP  
17 CK\_M\_DDR0\_B\_DN  
17 CK\_M\_DDR1\_B\_DP  
17 CK\_M\_DDR1\_B\_DN

## DDR OTHERS

15,17 DDR3\_DRAMRST\_N

U27A

1 OF 11

M\_MAA\_A0 AW27 SA\_MA\_0  
M\_MAA\_A1 AW24 SA\_MA\_1  
M\_MAA\_A2 AW24 SA\_MA\_2  
M\_MAA\_A3 AW23 SA\_MA\_3  
M\_MAA\_A4 AW23 SA\_MA\_4  
M\_MAA\_A5 AT24 SA\_MA\_5  
M\_MAA\_A6 AT23 SA\_MA\_6  
M\_MAA\_A7 AL22 SA\_MA\_7  
M\_MAA\_A8 AW22 SA\_MA\_8  
M\_MAA\_A9 AT22 SA\_MA\_9  
M\_MAA\_A10 AW28 SA\_MA\_10  
M\_MAA\_A11 AL21 SA\_MA\_11  
M\_MAA\_A12 AT21 SA\_MA\_12  
M\_MAA\_A13 AW22 SA\_MA\_13  
M\_MAA\_A14 AW20 SA\_MA\_14  
M\_MAA\_A15 AT20 SA\_MA\_15  
M\_WE\_A\_N AW23 SA\_WE#  
M\_CAS\_A\_N AW20 SA\_CAS#  
M\_RAS\_A\_N AL23 SA\_RAS#  
M\_SBS\_A0 AW29 SA\_BS\_0  
M\_SBS\_A1 AW28 SA\_BS\_1  
M\_SBS\_A2 AW20 SA\_BS\_2  
M\_SCS\_A\_N0 AL29 SA\_CSF\_0  
M\_SCS\_A\_N1 AW22 SA\_CSF\_1  
M\_SCKE\_A0 AW19 SA\_CKE\_0  
M\_SCKE\_A1 AW18 SA\_CKE\_1  
M\_COT\_A0 AW21 SA\_COT\_0  
M\_COT\_A1 AW22 SA\_COT\_1  
CK\_M\_DDR0\_A\_DP AW25 SA\_CK\_0  
CK\_M\_DDR0\_A\_DN AW25 SA\_CK\_0  
CK\_M\_DDR1\_A\_DP AL26 SA\_CK\_1  
CK\_M\_DDR1\_A\_DN AW27 SA\_CK\_2  
M\_SCKE\_B0 AW26 SA\_CK\_3  
M\_SCKE\_B1 AW26 SA\_CK\_3  
M\_COT\_B0 AW26 SA\_CK\_3  
M\_COT\_B1 AW26 SA\_CK\_3

DDR3\_DRAMRST\_N 1 R637 2 DDR3\_DRAMRST\_N-1 AW19 SM\_DRAMRST#  
SCDIU10V2KX4GP OR0402-PAD-2-GP

C474  
SCDIU10V2KX4GP

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

U27B

2 OF 11

M\_MAA\_B0 AK24 SB\_MA\_0  
M\_MAA\_B1 AM20 SB\_MA\_1  
M\_MAA\_B2 AM19 SB\_MA\_2  
M\_MAA\_B3 AK18 SB\_MA\_3  
M\_MAA\_B4 AP19 SB\_MA\_4  
M\_MAA\_B5 AP18 SB\_MA\_5  
M\_MAA\_B6 AM18 SB\_MA\_6  
M\_MAA\_B7 AL18 SB\_MA\_7  
M\_MAA\_B8 AN18 SB\_MA\_8  
M\_MAA\_B9 AM17 SB\_MA\_9  
M\_MAA\_B10 AN23 SB\_MA\_10  
M\_MAA\_B11 AU17 SB\_MA\_11  
M\_MAA\_B12 AT18 SB\_MA\_12  
M\_MAA\_B13 AR26 SB\_MA\_13  
M\_MAA\_B14 AT16 SB\_MA\_14  
M\_MAA\_B15 AV16 SB\_MA\_15  
M\_WE\_B\_N AR25 SB\_WE#  
M\_CAS\_B\_N AK25 SB\_CAS#  
M\_RAS\_B\_N AP24 SB\_RAS#  
M\_SBS\_B0 AP23 SB\_BS\_0  
M\_SBS\_B1 AM24 SB\_BS\_1  
M\_SBS\_B2 AW17 SB\_BS\_2  
M\_SCS\_B\_N0 AR25 SB\_CSF\_0  
M\_SCS\_B\_N1 AR25 SB\_CSF\_1  
M\_SCKE\_B0 AU16 SB\_CKE\_0  
M\_SCKE\_B1 AW15 SB\_CKE\_1  
M\_COT\_B0 AL26 SB\_COT\_0  
M\_COT\_B1 AP25 SB\_COT\_1  
CK\_M\_DDR0\_B\_DP AL21 SB\_CK\_0  
CK\_M\_DDR0\_B\_DN AL22 SB\_CK\_0  
CK\_M\_DDR1\_B\_DP AL20 SB\_CK\_1  
CK\_M\_DDR1\_B\_DN AK20 SB\_CK\_1  
M\_SCKE\_B0 AL23 SB\_CK\_2  
M\_SCKE\_B1 AL23 SB\_CK\_3  
M\_COT\_B0 AL23 SB\_CK\_3  
M\_COT\_B1 AL23 SB\_CK\_3

DDR3\_DRAMRST\_N 1 R637 2 DDR3\_DRAMRST\_N-1 AW19 SM\_DRAMRST#  
SCDIU10V2KX4GP OR0402-PAD-2-GP

C474  
SCDIU10V2KX4GP

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

<Variant Name>

wistron

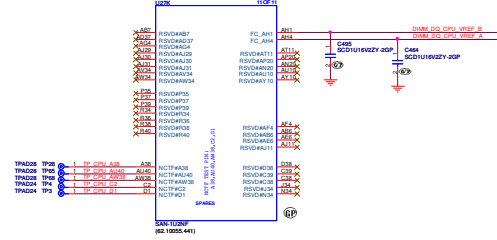
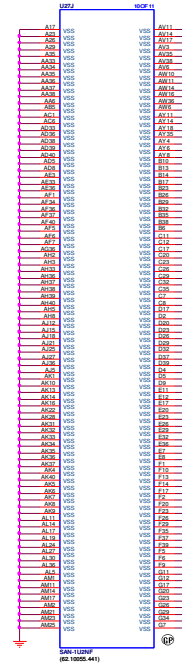
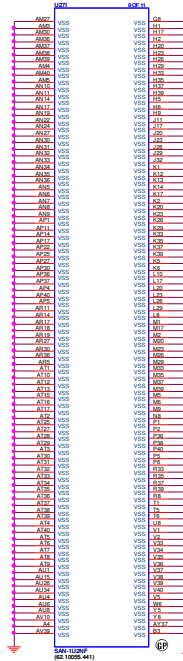
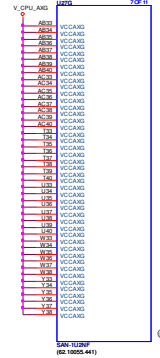
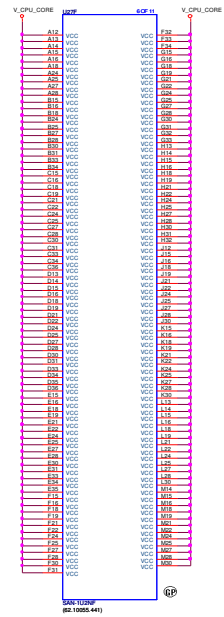
Wistron Incorporated  
21F, 88, Hein Tai Wu Rd  
Hsichih, Taipei

Title

Size C Document Number New Mission Hills

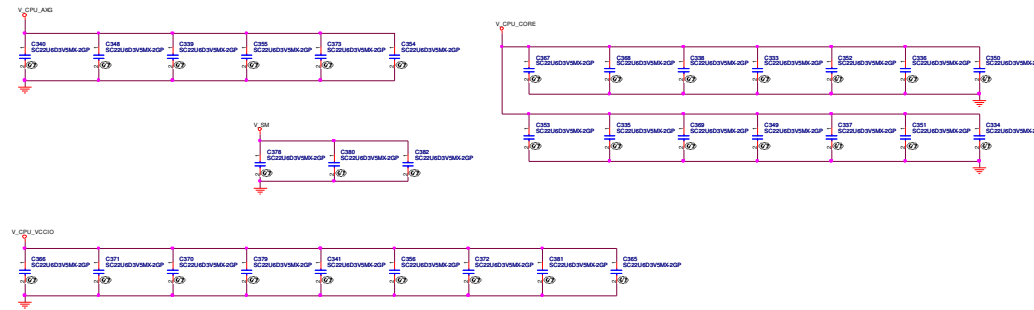
Date: Sunday, March 20, 2011 Sheet 12 of 51

17 DIMM DQ CPU\_VREF\_B  
15 DIMM DQ CPU\_VREF\_A

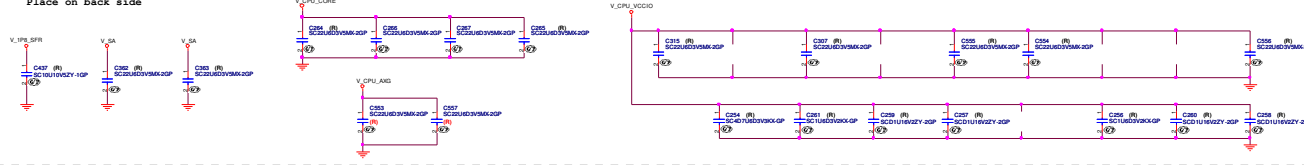


Net	CAP	AMOUNT
Vcore	22uf 0805	14+4
VCCIO	22uf 0805	9+16 (R)
V_AXG	22uf 0805	4+2 (R)
VCCSA	10uf 0805	2+0
VDDQ	22uf 0805	9
VCCPLL	10uf 0805	1

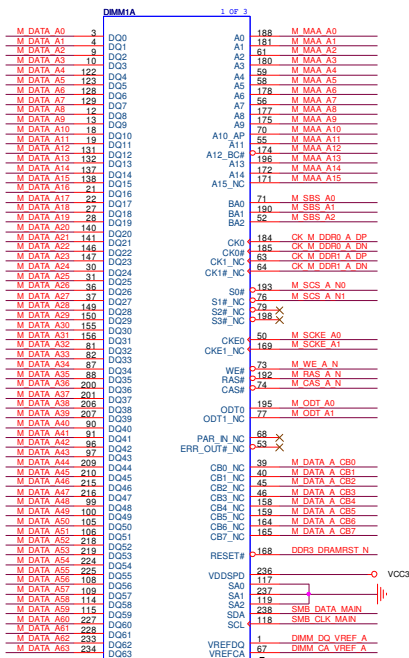
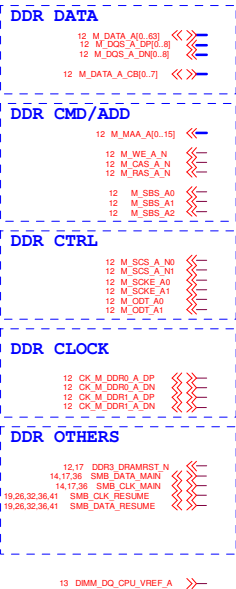
Place in the CPU Cavity Area

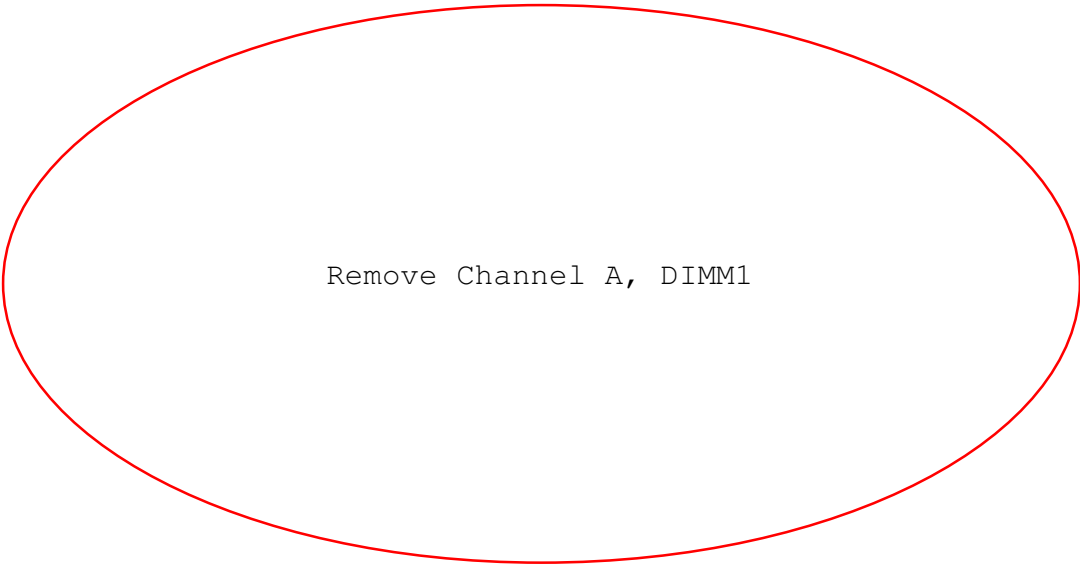


Place on back side

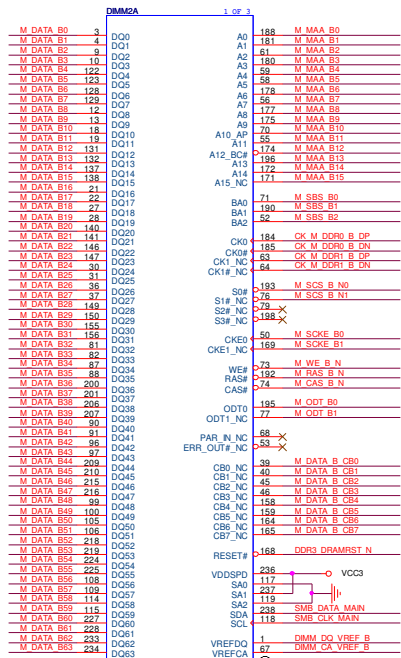
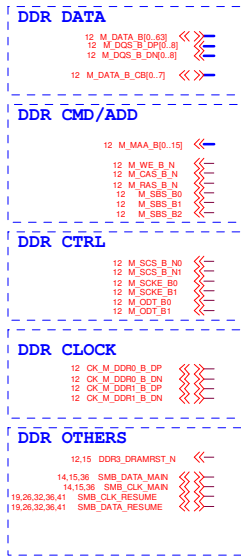


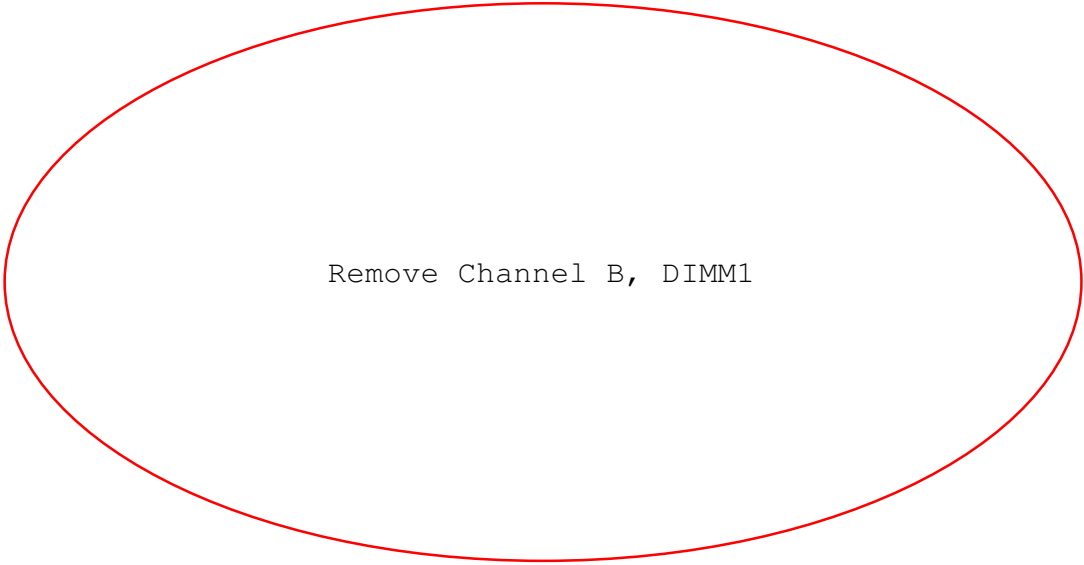




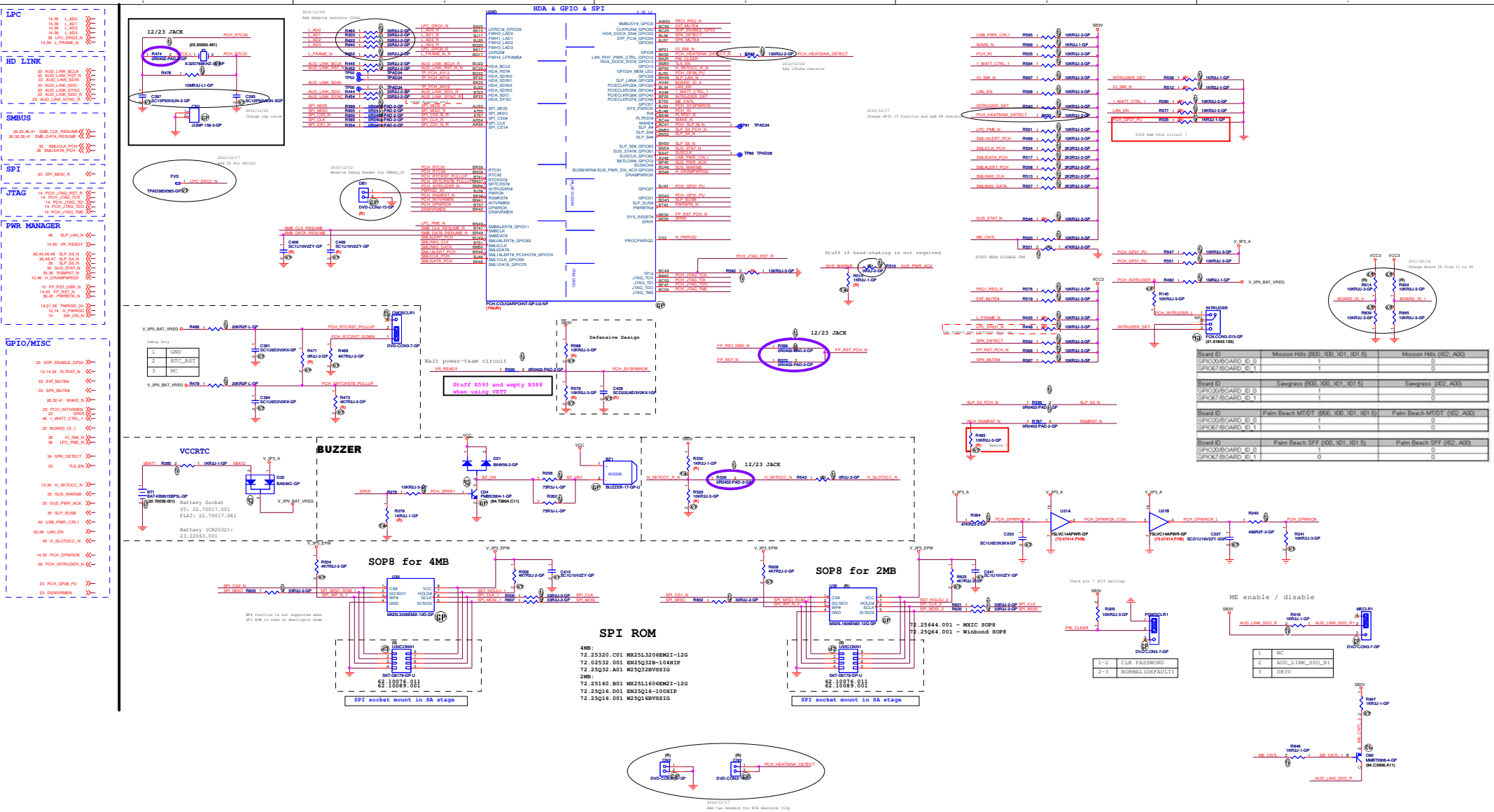








Remove Channel B, DIMM1



Board ID	Mission Hills (200, 300, 301, 301.5)	Mission Hills (402, 400)
GPIO0/BOARD_ID_0	1	0
GPIO67/BOARD_ID_1	1	0

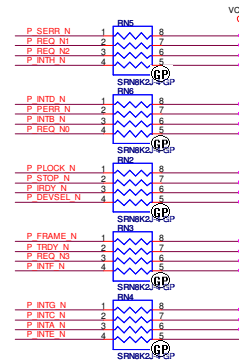
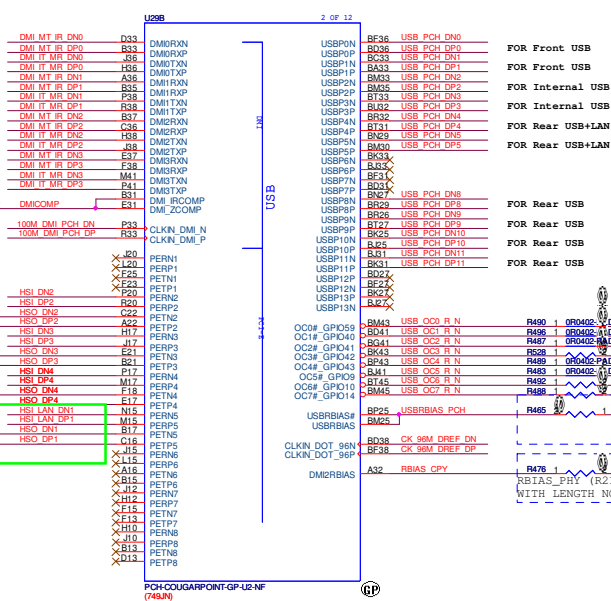
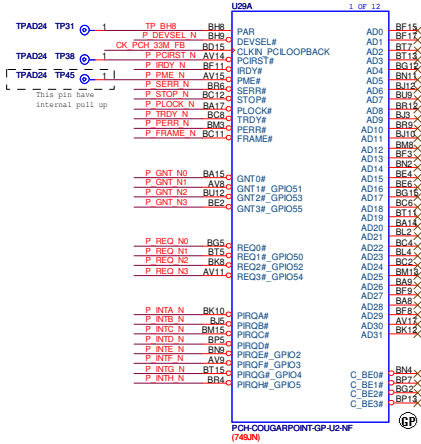
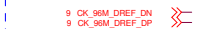
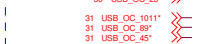
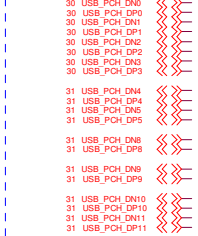
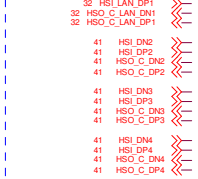
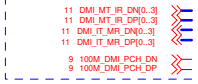
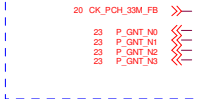
Board ID	Sawgrass (300, 300, 301, 301.5)	Sawgrass (402, 400)
GPIO0/BOARD_ID_0	1	0
GPIO67/BOARD_ID_1	1	0

Board ID	Palm Beach MT/OT (300, 300, 301, 301.5)	Palm Beach MT/OT (402, 400)
GPIO0/BOARD_ID_0	1	0
GPIO67/BOARD_ID_1	1	0

Board ID	Palm Beach SFF (300, 301, 301.5)	Palm Beach SFF (402, 400)
GPIO0/BOARD_ID_0	1	0
GPIO67/BOARD_ID_1	1	0







OC[0..3] for Ports 0-7  
OC[4..7] for Ports 8-13

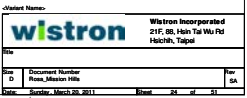
R488 10K B2J-3-GP

R465 22D6R2-L-1-GP

USBRBIAS (R63LB): TIE TRACES TOGETHER CLOSE TO PINS, WITH LENGTH NO LONGER THAN 450 MILS TO

RBIAS\_PHY (R211LB): TIE TRACES TOGETHER CLOSE TO PINS,  
WITH LENGTH NO LONGER THAN 450 MILS TO RESISTOR

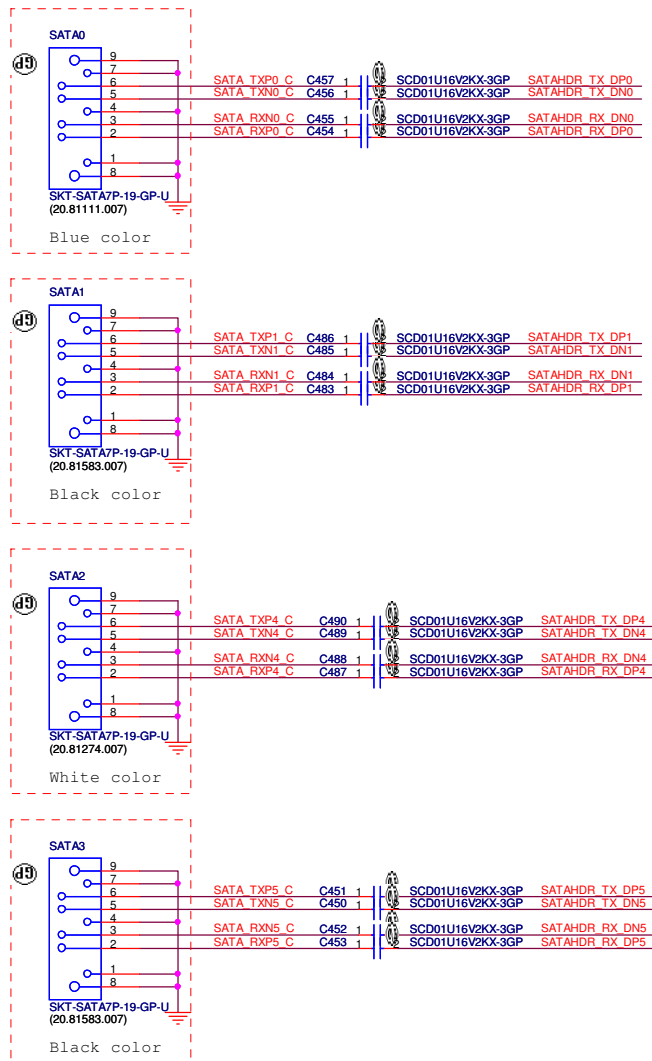






# SATA

21 SATAHDR\_RX\_DP0 <<=  
 21 SATAHDR\_RX\_DN0 >>=  
 21 SATAHDR\_TX\_DN0 >>=  
 21 SATAHDR\_TX\_DP0 >>=  
 21 SATAHDR\_RX\_DP1 <<=  
 21 SATAHDR\_RX\_DN1 >>=  
 21 SATAHDR\_TX\_DN1 >>=  
 21 SATAHDR\_TX\_DP1 >>=  
 21 SATAHDR\_RX\_DP4 <<=  
 21 SATAHDR\_RX\_DN4 >>=  
 21 SATAHDR\_TX\_DN4 >>=  
 21 SATAHDR\_TX\_DP4 >>=  
 21 SATAHDR\_RX\_DP5 <<=  
 21 SATAHDR\_RX\_DN5 >>=  
 21 SATAHDR\_TX\_DN5 >>=  
 21 SATAHDR\_TX\_DP5 >>=



NOTE:

PCH only port 0&1 support SATA 3.0

<Variant Name>

<b>wistron</b>		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title			
Size A3	Document Number Rosa_Mission Hills	Rev SA	
Date: Sunday, March 20, 2011	Sheet 25	of 51	

# PCIEX16

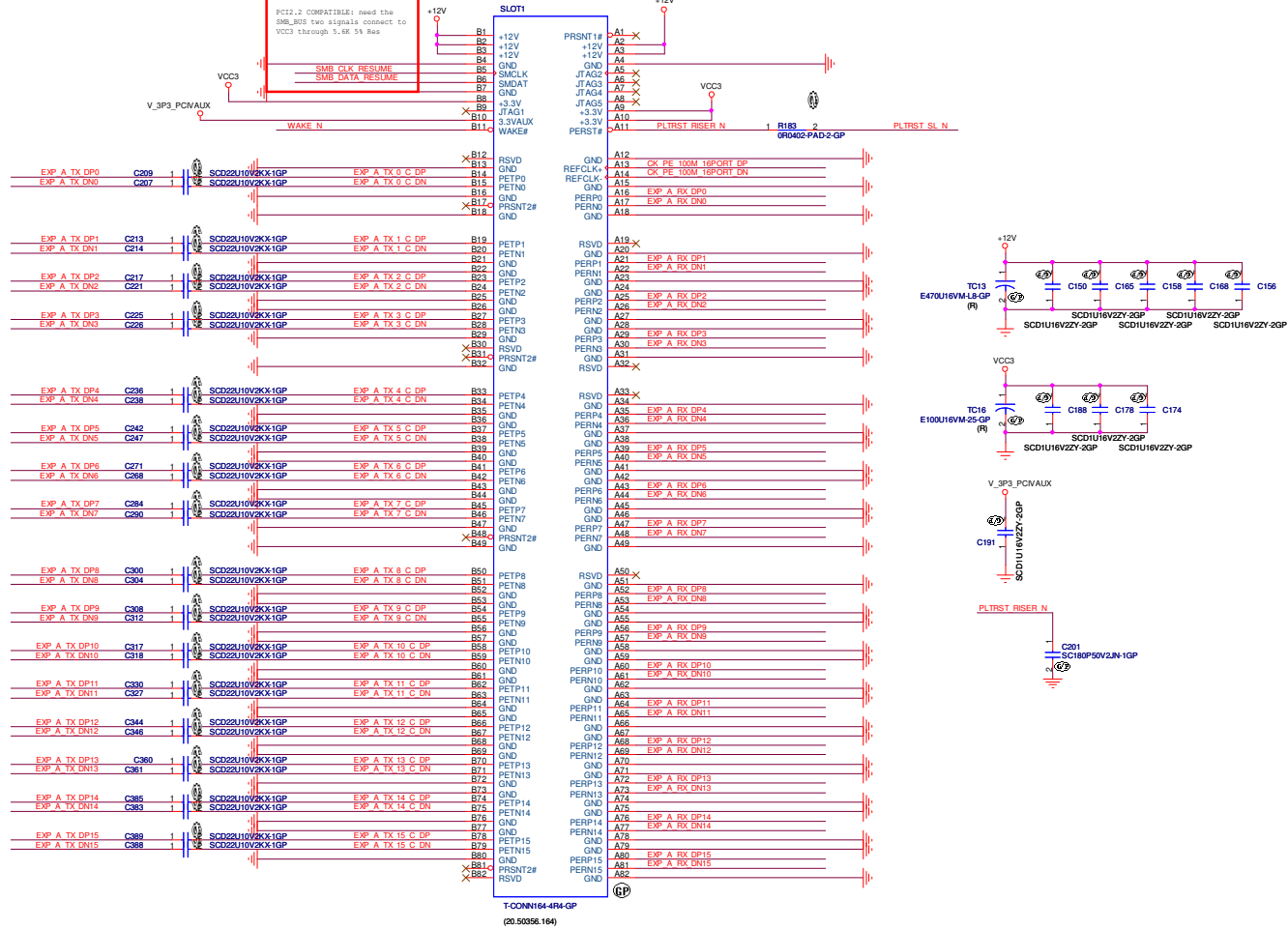
11 EXP\_A\_RX\_DN0..15  
11 EXP\_A\_TX\_DP0..15  
11 EXP\_A\_TX\_DP10..15  
11 EXP\_A\_TX\_DP15..15  
20 CK\_PE\_100M\_1PORT\_DP  
20 CK\_PE\_100M\_1PORT\_DN  
14.38 PLTRST\_SL\_N

# OTHERS

19.32.36.41 SMB\_CLK\_RESUME  
19.32.36.41 SMB\_DATA\_RESUME  
19.32.41 WAKE\_N

w/o Latch: 20.50352.164  
with Latch: 20.50512.164, 20.50356.164

PCIEX16 CONN may need LATCH if supporting 75W GFX Card



<Variant Name>

<b>wistron</b>		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Heichih, Taipei	
Title			
Size	Document Number	Rev	
C	Rosa_Mission Hills	SA	
Date:	Sunday, March 20, 2011	Sheet	28 of 51

# RGB

21 VGA\_RED  
21 VGA\_GREEN  
21 VGA\_BLUE

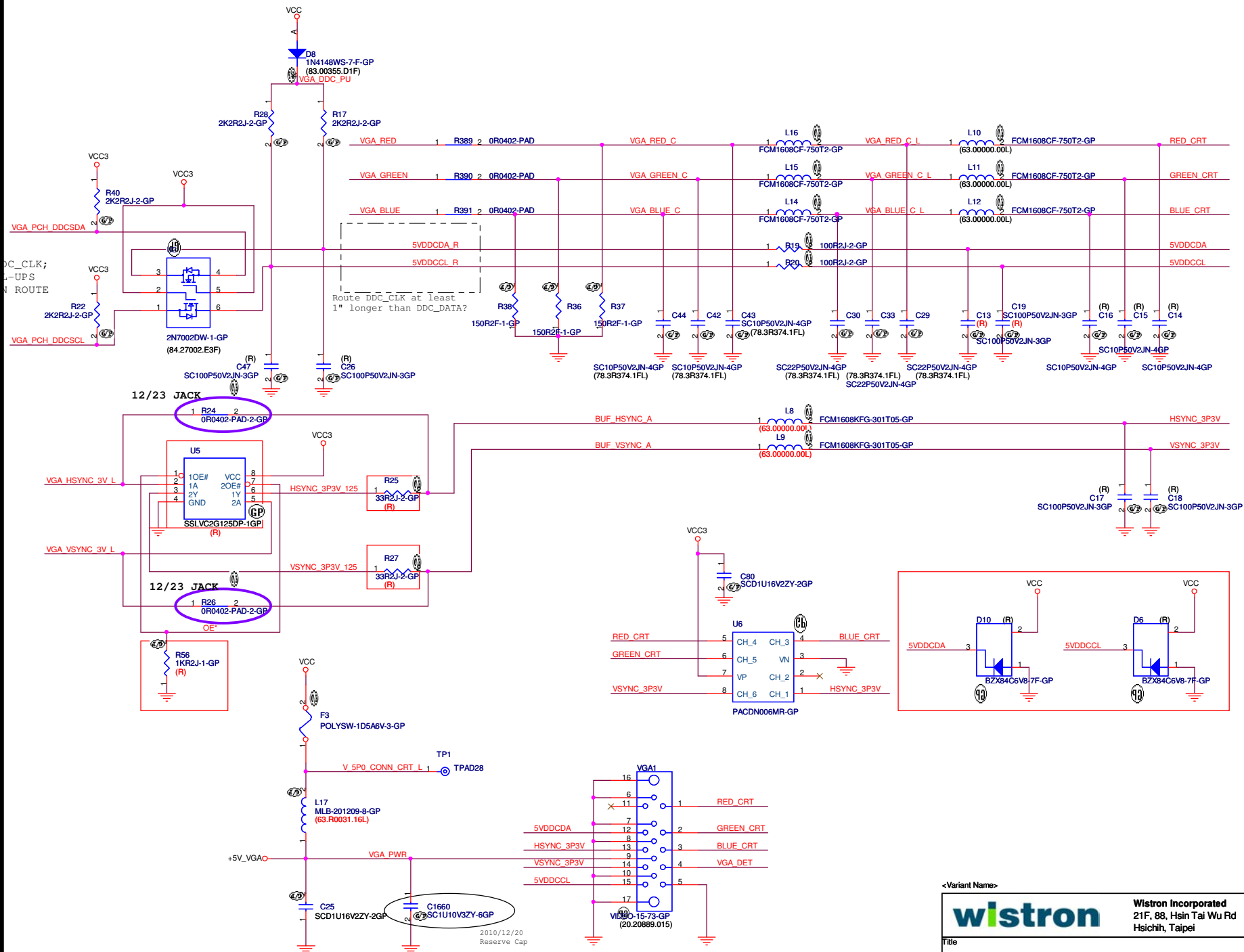
# SYNC

21 VGA\_HSYNC\_3V\_L  
21 VGA\_VSYNC\_3V\_L

# DDC

21 VGA\_PCH\_DDCSDA  
21 VGA\_PCH\_DDCSCL  
21 VGA\_DET

DDC\_DATA/DDC\_CLK;  
LOCATE PULL-UPS  
ANYWHERE ON ROUTE  
OF TRACE



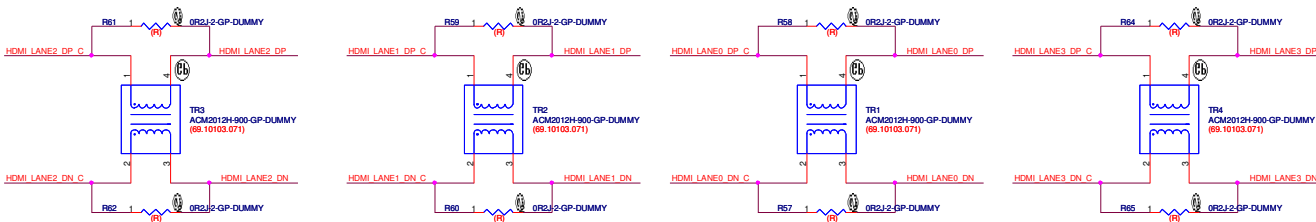
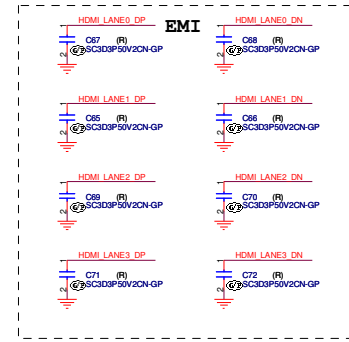
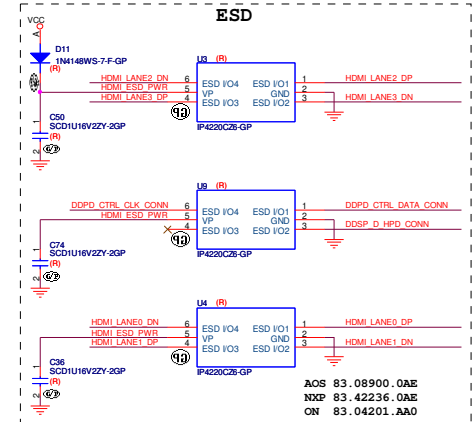
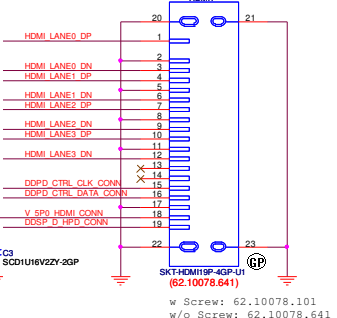
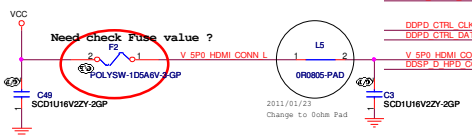
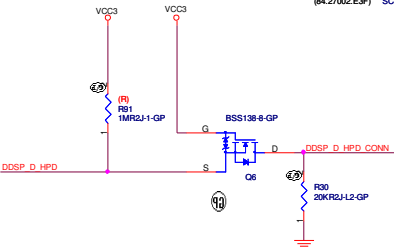
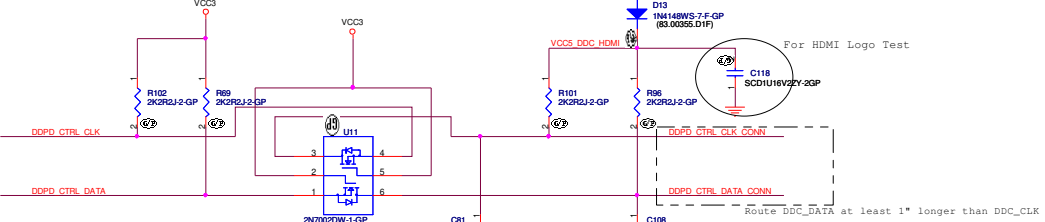
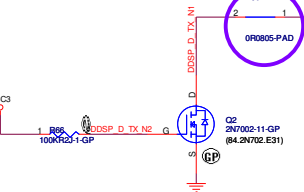
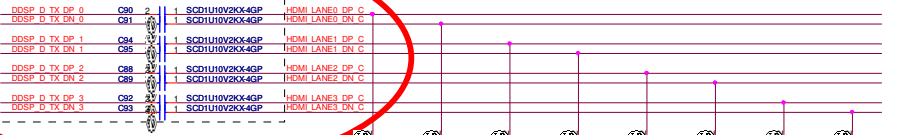
<Variant Name>

<b>wistron</b>			<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title			
Size A3	Document Number Rosa_Mission Hills		Rev SA
Date:	Sunday, March 20, 2011	Sheet	27 of 51

# DVI PORT

21 DDSP\_D\_TX\_DP\_0  
21 DDSP\_D\_TX\_DN\_0  
21 DDSP\_D\_TX\_DP\_1  
21 DDSP\_D\_TX\_DN\_1  
21 DDSP\_D\_TX\_DP\_2  
21 DDSP\_D\_TX\_DN\_2  
21 DDSP\_D\_TX\_DP\_3  
21 DDSP\_D\_TX\_DN\_3  
21 DDSP\_D\_TX\_CLK  
21 DDSP\_CTRL\_DATA  
21 DDSP\_D\_HPD

## PCH PORT D Place near HDMI Connector



DISPLAY PORT

RESERVED

<Variant Name>

**wistron**

**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsinchu, Taipei

Title

Size  
C

Document Number  
Rosa\_Mission Hills

Rev  
SA

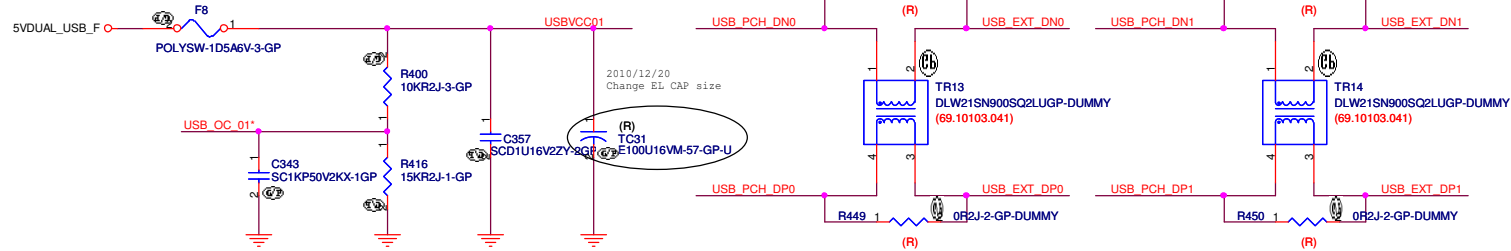
Date: Sunday, March 20, 2011

Sheet 20 of 51

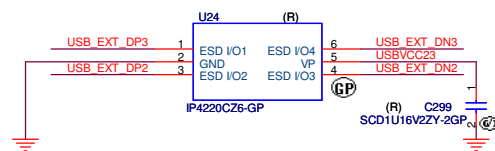
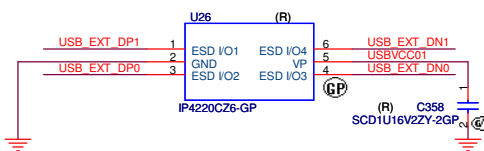
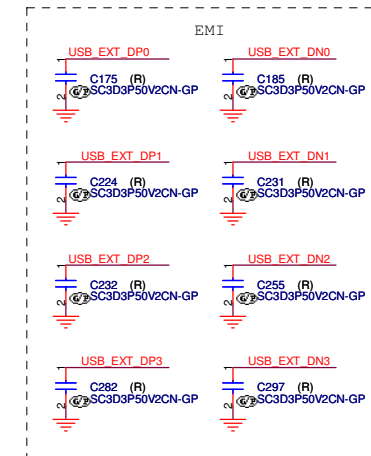
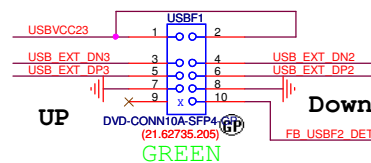
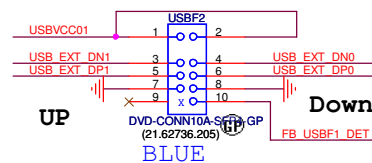
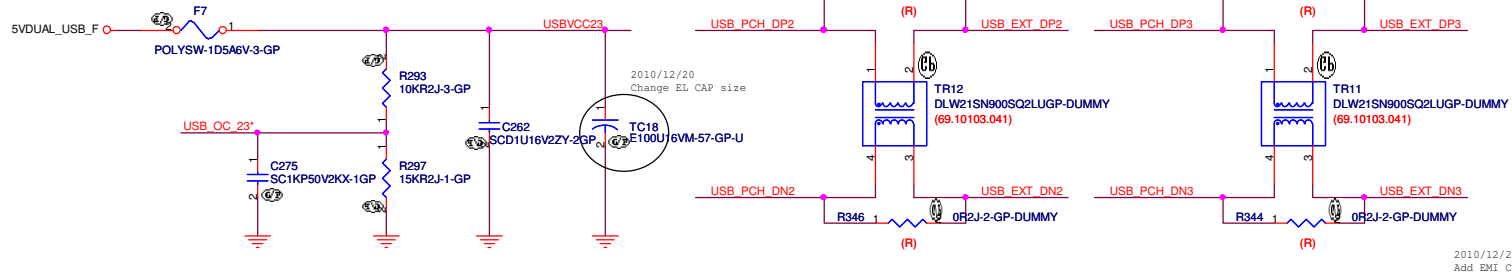
# FRONT USB

- 22 USB\_PCH\_DP0
- 22 USB\_PCH\_DN0
- 22 USB\_PCH\_DP1
- 22 USB\_PCH\_DN1
- 22 USB\_OC\_01\*
- 21 FB\_USBF1\_DET
- 22 USB\_PCH\_DP2
- 22 USB\_PCH\_DN2
- 22 USB\_PCH\_DP3
- 22 USB\_PCH\_DN3
- 22 USB\_OC\_23\*
- 21 FB\_USBF2\_DET
- 22,31 USB\_PCH\_DN10
- 22,31 USB\_PCH\_DP10
- 22,31 USB\_PCH\_DN11
- 22,31 USB\_PCH\_DP11

## FRONT USB PORT



## FRONT USB PORT



```

22 USB_PCH_DP4
22 USB_PCH_DP4
22 USB_PCH_DP5
22 USB_PCH_DP5

32 LAN_MDIO2_DP
32 LAN_MDIO2_DN
32 LAN_MDIO1_DP
32 LAN_MDIO1_DN
32 LAN_MDIO0_DP
32 LAN_MDIO0_DN
32 LAN_MDIO3_DP
32 LAN_MDIO3_DN

32 SPEED_100_N
32 SPEED_1000_N
32 LINK_ACTIVITY_N

```

22 USB\_PCH\_DP8

22 USB\_PCH\_DN8

22 USB\_PCH\_DP9

22 USB\_PCH\_DN9

22 USB\_PCH\_DP10

22 USB\_PCH\_DN10

22 USB\_PCH\_DP11

22 USB\_PCH\_DN11

22 USB\_OC\_89\*

22 USB\_OC\_45\*

22 USB\_OC\_1011\*

## REAR USB

[illegible][illegible][illegible][illegible]

	Giga	100	10
Link	Orange	Green	X
Act	Blink	Blink	Blink

EMI

LAN WDS DP	LAN WDS CN	LAN WDS DP	LAN WDS CN	LAN WDS DP	LAN WDS CN	LAN WDS DP	LAN WDS CN
C116 南 ②GND③P5V2XON-GP	C115 南 ②GND③P5V2XON-GP	C114 南 ②GND③P5V2XON-GP	C113 南 ②GND③P5V2XON-GP	C112 南 ②GND③P5V2XON-GP	C111 南 ②GND③P5V2XON-GP	C110 南 ②GND③P5V2XON-GP	C109 南 ②GND③P5V2XON-GP

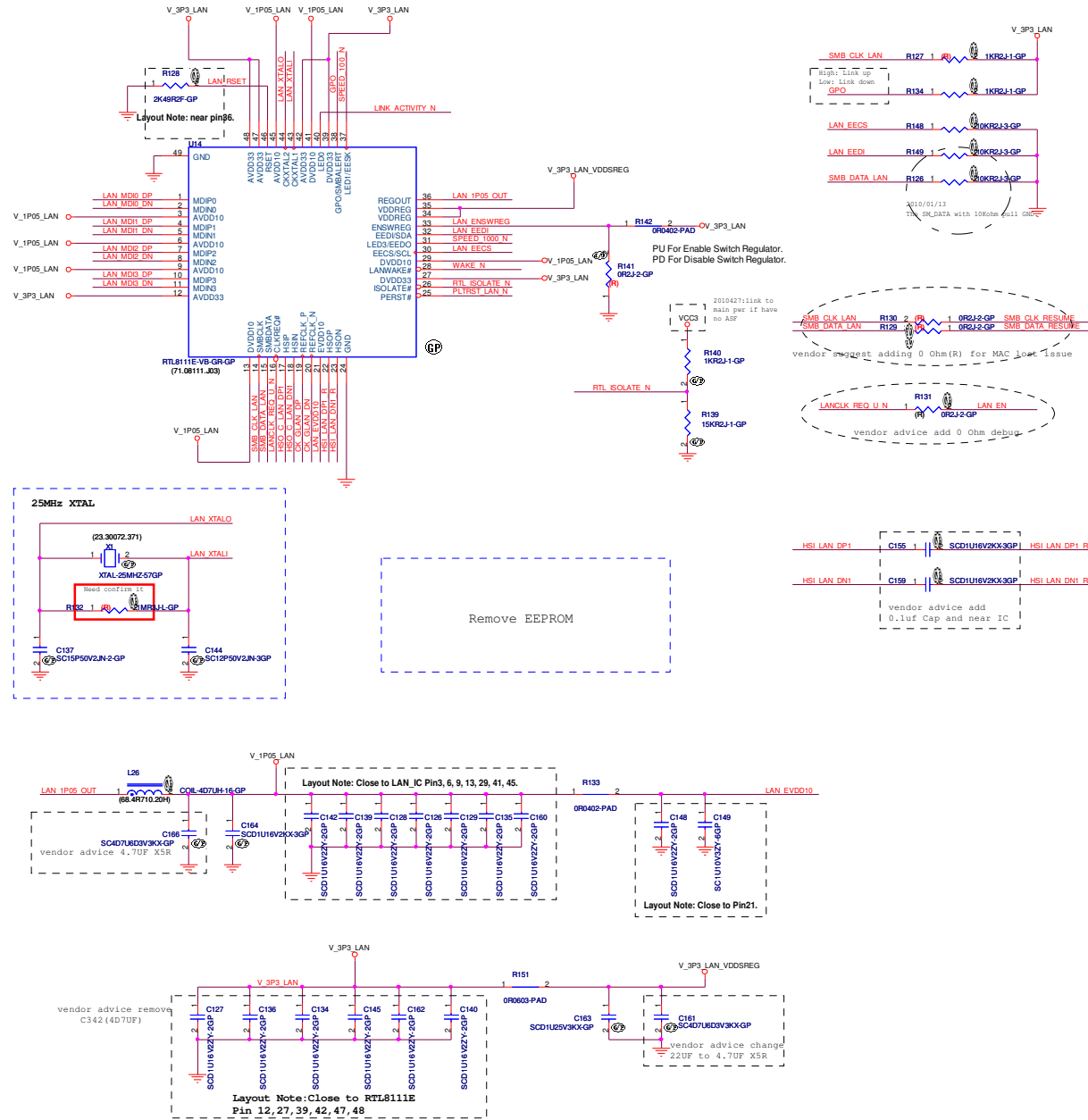
[illegible]

## To connector

31 LAN\_MDIO\_DP  
31 LAN\_MDIO\_DN  
31 LAN\_MDIO\_DP  
31 LAN\_MDIO\_DN  
31 LAN\_MDIO\_DP  
31 LAN\_MDIO\_DN  
31 LAN\_MDIO\_DP  
31 LAN\_MDIO\_DN  
31 SPEED\_100\_N  
31 SPEED\_1000\_N  
31 LINK\_ACTIVITY\_N

## OTHERS

20 CK\_GLAN\_DP  
20 CK\_GLAN\_DN  
22 HSI\_LAN\_DP1  
22 HSI\_LAN\_DN1  
22 HSD\_C\_LAN\_DP1  
22 HSD\_C\_LAN\_DN1  
19,28,35,41 SMB\_CLK\_RESUME  
19,28,36,41 SMB\_DATA\_RESUME  
19,46 LAN\_EN  
36 PLTRST\_LAN\_N  
19,26,41 WAKE\_N



<Variant Name>

**wistron**

Wistron Incorporated  
21F, 88, Hein Tai Wu Rd  
Hsichih, Taipei

Title

Size

Document Number  
Pss\_Mission Hills

C

Date

Sheet

32 of 51

SA



## HD\_LINK

19 AUD\_LINK\_SDN  
19 AUD\_LINK\_SDO  
19 AUD\_LINK\_RST\_N  
19 AUD\_LINK\_SYNC  
19 AUD\_LINK\_BCLK

## Rear I/O

LINE-OUT  
34 LOUT\_R  
34 LOUT\_L  
34 LOUT\_ID

LINE-IN  
34 LIN\_R  
34 LIN\_L  
34 LIN\_ID

MIC-IN  
34 MIC\_IN\_R  
34 MIC\_IN\_L  
34 MIC\_ID  
34 MIC1\_VREF0

## Front I/O

HP-OUT  
34 FP\_OUT\_L  
34 FP\_OUT\_R  
34 LINE2\_ID

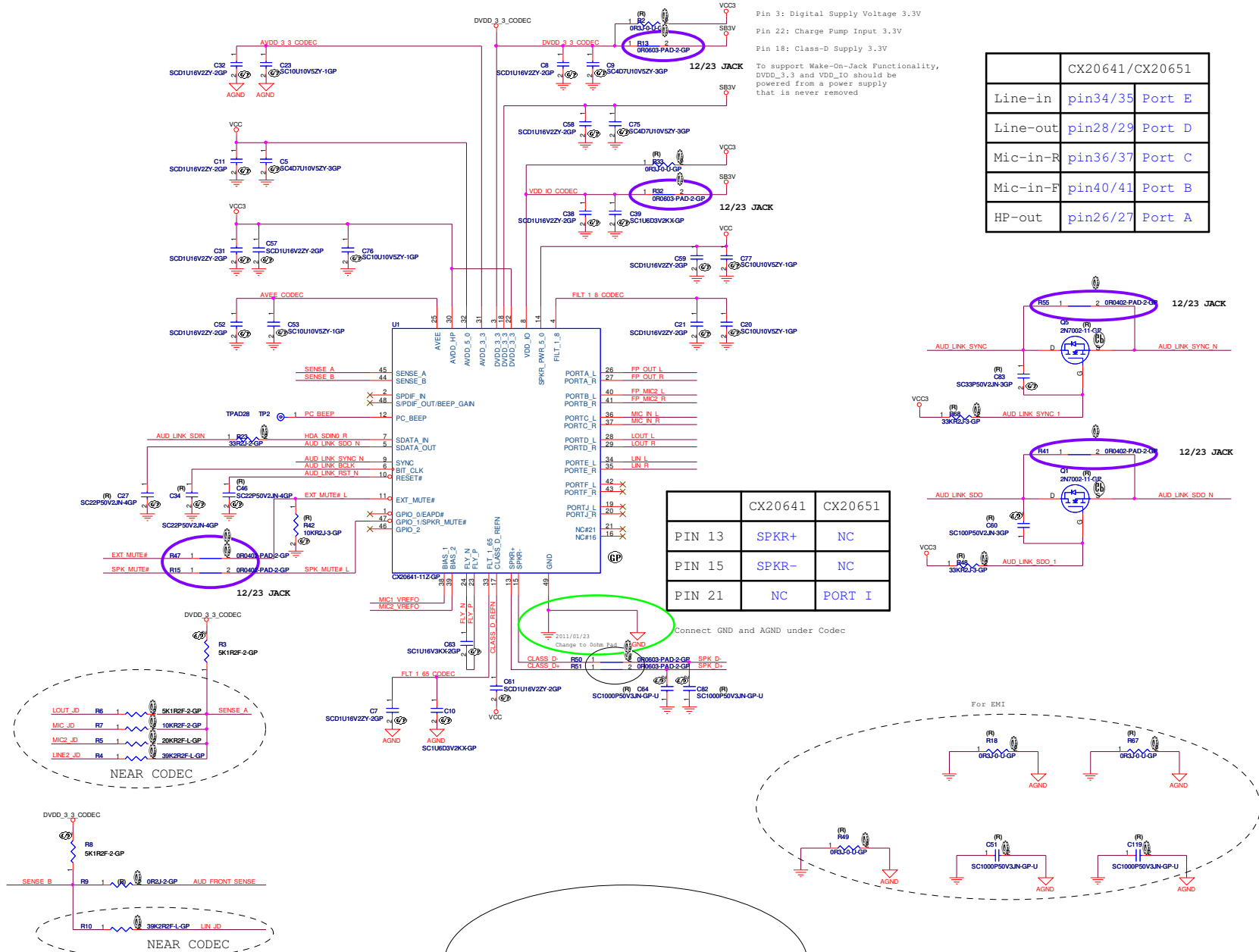
MIC-IN  
34 FP\_MIC2\_R  
34 FP\_MIC2\_L  
34 MIC2\_ID  
34 MIC2\_VREF0

## Internal Speaker

34 SPK\_D-  
34 SPK\_D+

## Others

34 AUD\_FRONT\_SENSE  
19 EXT\_MUTE#  
19 SPK\_MUTE#



Pin 3: Digital Supply Voltage 3.3V  
Pin 22: Charge Pump Input 3.3V  
Pin 18: Class-D Supply 3.3V  
To support Wake-On-Jack Functionality, DVDD\_3.3 and VDD\_IO should be powered from a power supply that is never removed

	CX20641/CX20651
Line-in	pin34/35 Port E
Line-out	pin28/29 Port D
Mic-in-R	pin36/37 Port C
Mic-in-F	pin40/41 Port B
HP-out	pin26/27 Port A

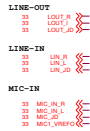
	CX20641	CX20651
PIN 13	SPKR+	NC
PIN 15	SPKR-	NC
PIN 21	NC	PORT I

2011/01/23  
Change to Dots Pad  
Connect GND and AGND under Codec

For EMI

Remove De-Pop Circuit

Rear I/O



Front I/O



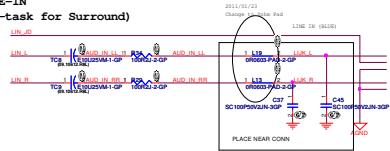
SPEAKER



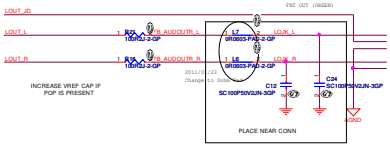
Others



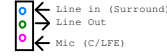
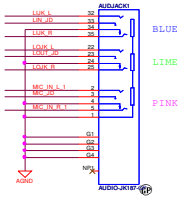
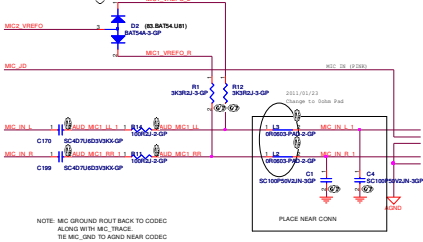
LINE-IN  
(Re-task for Surround)



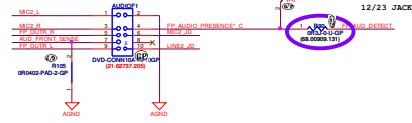
LINE-OUT



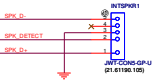
MIC-IN  
(Re-task for C/LFE)



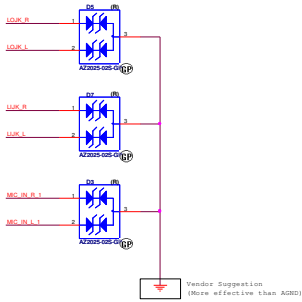
Front Panel



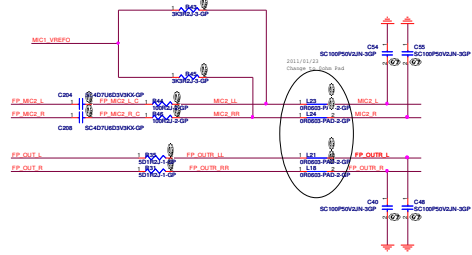
Internal Speaker

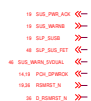


ESD

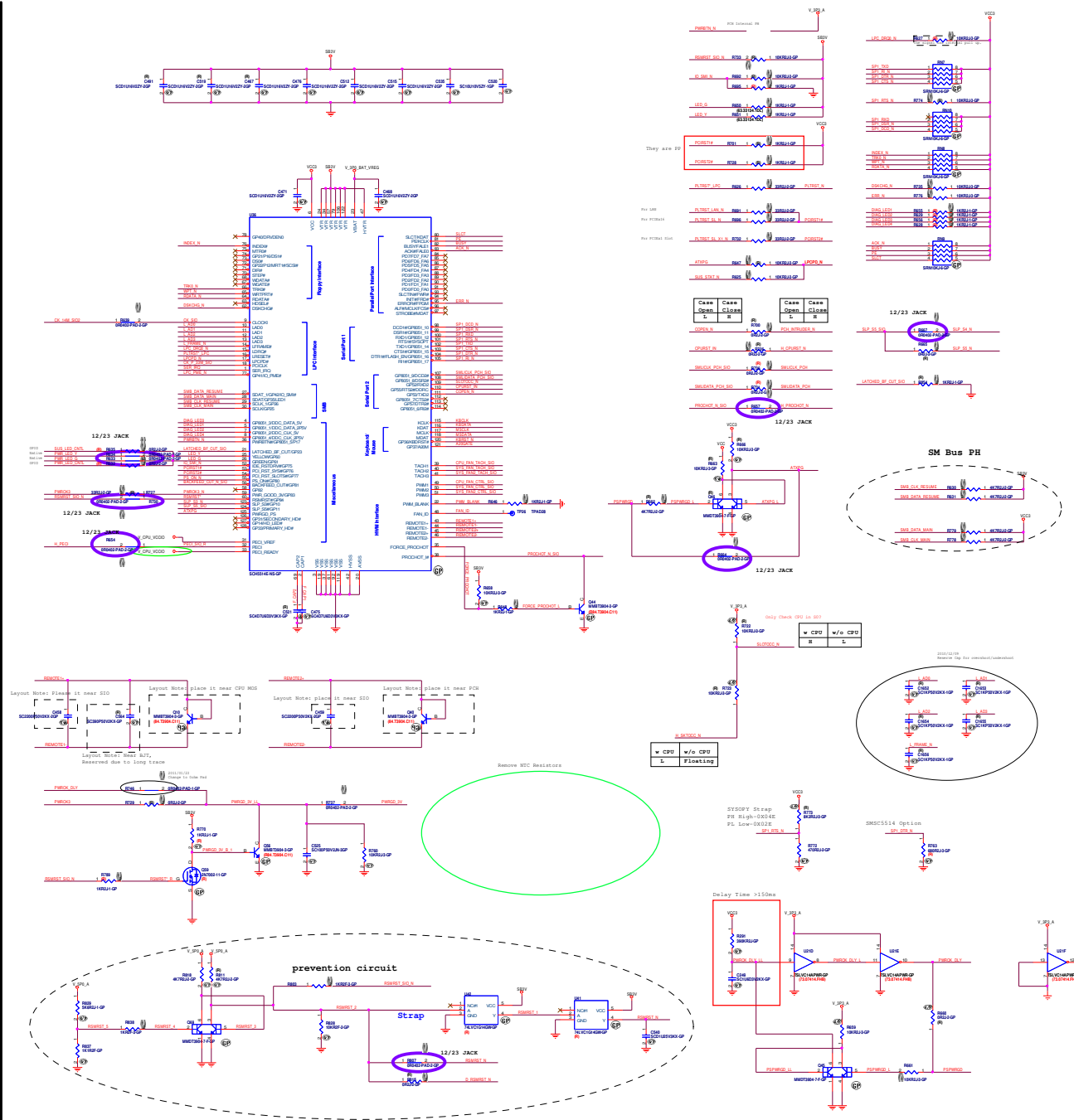


Remove Mute Circuit





<b>FAN</b>	14 FAN_PAN_TACH_S0
<b>CLOCK</b>	15 CLK_14M_S0
<b>LPC</b>	16 LPC_PAN_TACH_S0
<b>COM</b>	17 COM_PAN_TACH_S0
<b>SMBUS</b>	18 SMBUS_PAN_TACH_S0
<b>OTHERS</b>	19 OTHERS_PAN_TACH_S0
<b>Power Manager</b>	20 PM_PAN_TACH_S0
<b>PECI</b>	21 Peci_Pan_Tach_S0
<b>GPIO</b>	22 GPIO_Pan_Tach_S0
<b>KBMS</b>	23 KBMS_Pan_Tach_S0
<b>LED</b>	24 LED_Pan_Tach_S0

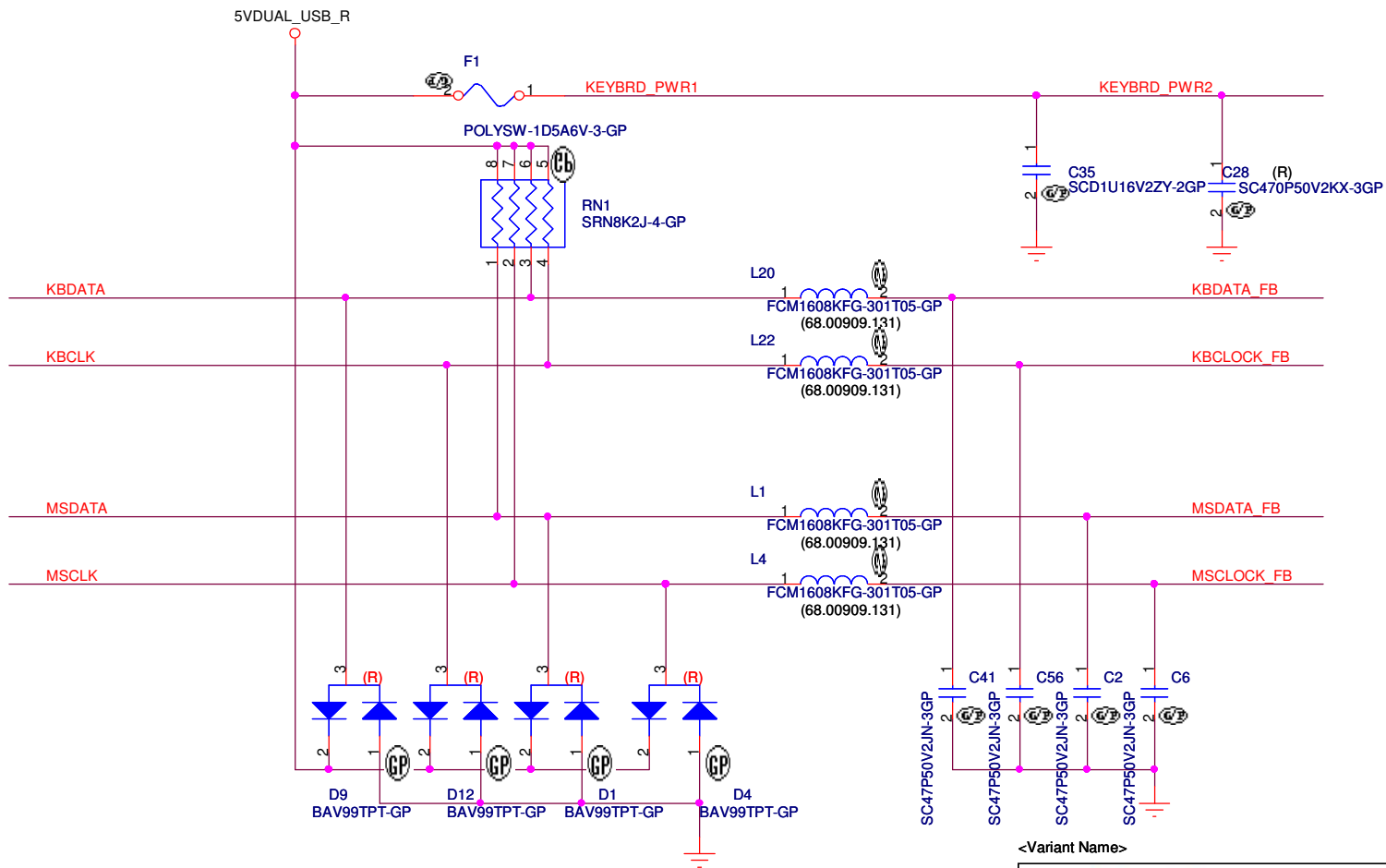


# PS2 KB/MS

36 KBDATA <<<<  
 36 KBCLK <<<<  
 36 MSDATA <<<<  
 36 MSCLK <<<<

38 KBDATA\_FB <<<<  
 38 KBCLOCK\_FB <<<<  
 38 MSDATA\_FB <<<<  
 38 MSCLOCK\_FB <<<<

38 KEYBRD\_PWR2 <<<<



**wistron**

**Wistron Incorporated**  
 21F, 88, Hsin Tai Wu Rd  
 Hsichih, Taipei

Title

Size  
A4

Document Number  
Rosa\_Mission Hills

Rev  
SA

Date: Sunday, March 20, 2011

Sheet 37 of 51

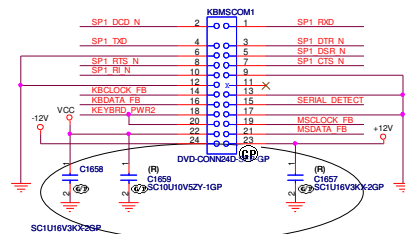
# COM Port

36 SP1\_RTS\_N <<<  
 36 SP1\_DTR\_N <<<  
 36 SP1\_DSR\_N <<<  
 36 SP1\_RXD <<<  
 36 SP1\_DCD\_N <<<  
 36 SP1\_TXD <<<  
 36 SP1\_CTS\_N <<<  
 36 SP1\_RL\_N <<<

21 SERIAL\_DETECT <<<

# KB/MS

37 KBDATA\_FB <<<  
 37 KBLOCK\_FB <<<  
 37 MSDATA\_FB <<<  
 37 MSLOCK\_FB <<<  
 37 KEYBRD\_PWR2 >>>



2010/12/20  
 Add cap for power noise

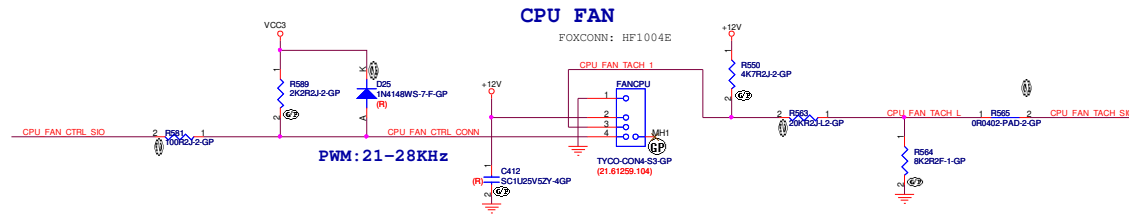
<Variant Name>

**wistron** Wistron Incorporated  
 21F, 88, Hein Tai Wu Rd  
 Hsichih, Taipei

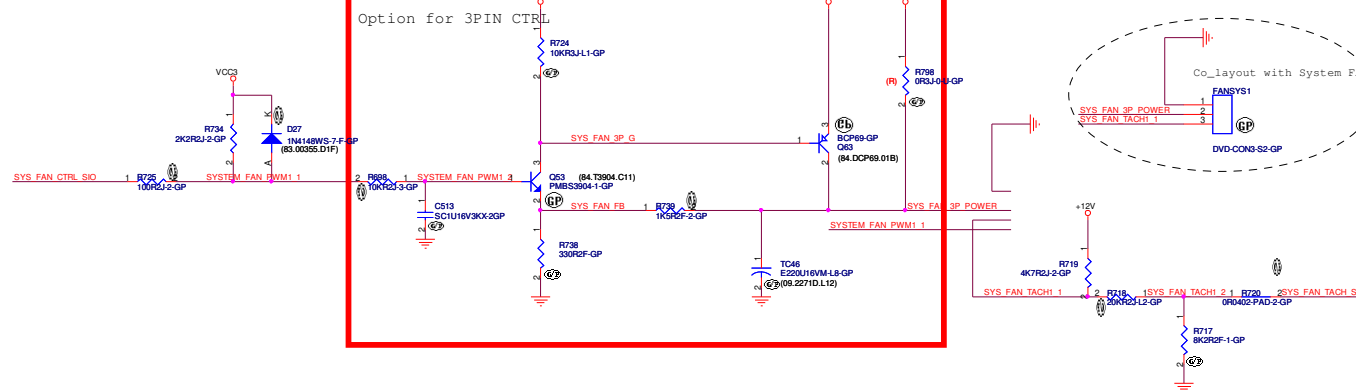
Title		
Size	Document Number	Rev
C	Pass_Mission Hills	SA
Date:	Sunday, March 20, 2011	Sheet 38 of 51

# SIO FAN CONTROL

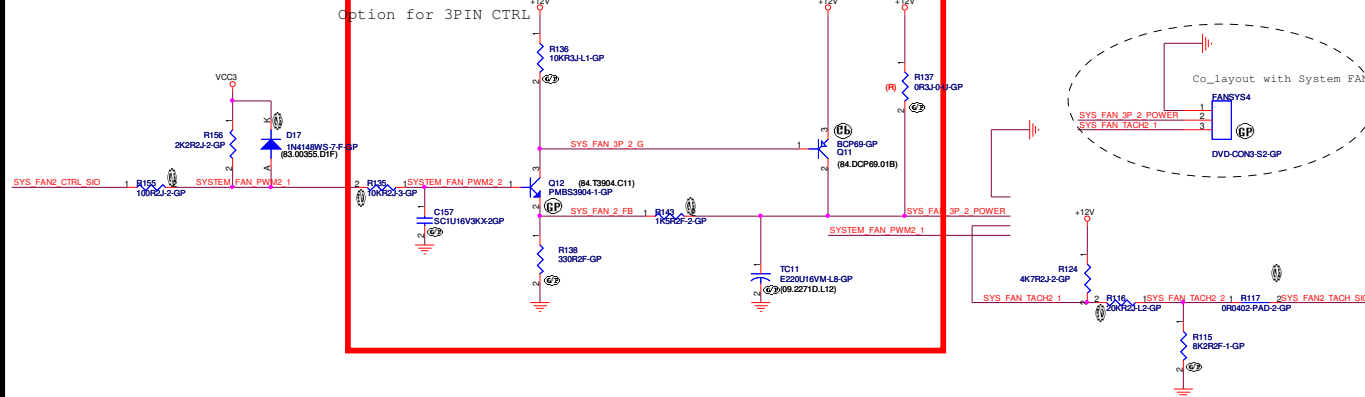
- 36 CPU\_FAN\_CTRL\_SIO
- 36 CPU\_FAN\_TACH\_SIO
- 36 SYS\_FAN\_CTRL\_SIO
- 36 SYS\_FAN\_TACH\_SIO
- 36 SYS\_FAN2\_CTRL\_SIO
- 36 SYS\_FAN2\_TACH\_SIO



## SYS 3 PINS/4 PINS FAN CONTROL

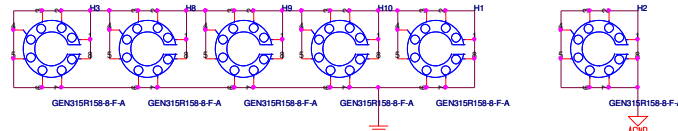
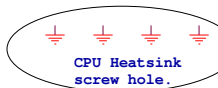


## 2nd SYS 3 PINS/4 PINS FAN CONTROL



## PCB MOUNTING HOLES

Remove CPU Heatsink Screw Holes




Variant Name:

<b>wistron</b>		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsinshih, Taipei
File	Document Number	Rev
Size	Customer/Mission Hubs	SA
Date: Sunday, March 20, 2011	Sheet 39 of 51	

	5	4	3	2	1	
D						D
C						C
B						B
A						A
	5	4	3	2		

RESERVED

<Variant Name>			
		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title			
Size B	Document Number Rosa_Mission Hills		Rev SA
Date:	Sunday, March 20, 2011	Sheet	40 of 51



ONFI

PCIEX1

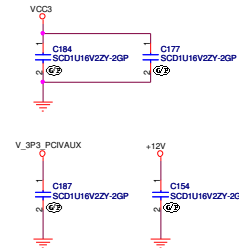
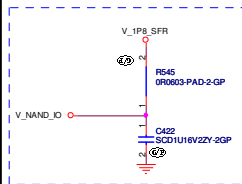
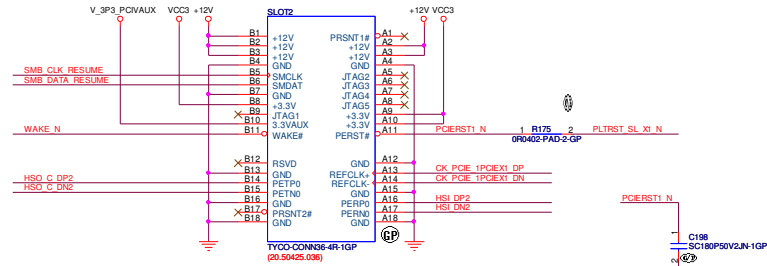
PCIEX1

PCIEX1

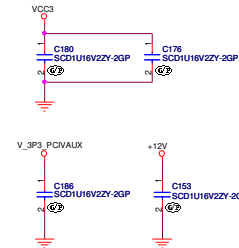
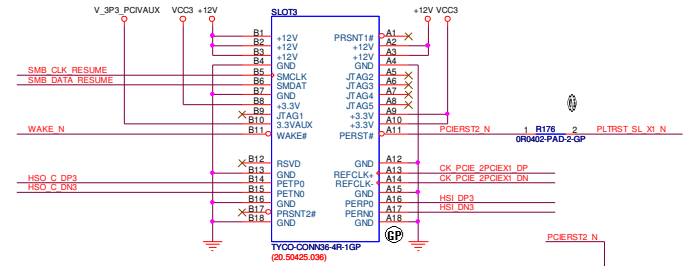
Others

35 PLTRST\_SL\_X1\_N  
19,26,32,36 SMB\_CLK\_RESUME  
19,26,32,36 SMB\_DATA\_RESUME  
19,26,32 SMB\_CLK\_RESUME  
19,26,32 SMB\_DATA\_RESUME  
19,26,32 WAKE\_N

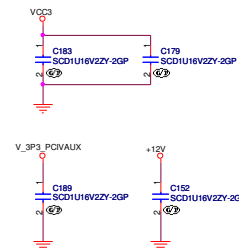
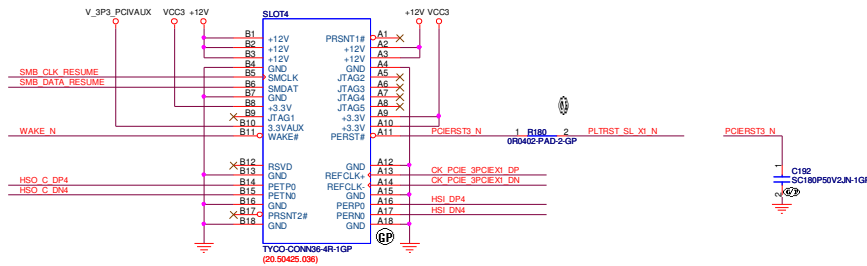
## PCIEX1 CONN



## PCIEX1 CONN



## PCIEX1 CONN



&lt;Variant Name&gt;

**wistron**

Wistron Incorporated  
21F, 88, Hei Tai Wu Rd  
Hsichih, Taipei

Title

Size

C

Date

Sunday, March 20, 2011

Sheet

41

of

51

SA

RESERVED

RESERVED

<Variant Name>

**wistron**

**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title

Size  
B

Document Number  
Rosa\_Mission Hills

Rev  
SA

Date: Sunday, March 20, 2011

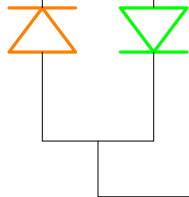
Sheet 43 of 51

RESERVED

```

36 DIAG_LED1    >>—
36 DIAG_LED2    >>—
36 DIAG_LED3    >>—
36 DIAG_LED4    >>—

```

[illegible]

Green LED

Prevent circuit

### NT PANEL HEADER

2010/10/21  
delete D29 diode

V<sub>5P0\_A</sub>

R699  
220R51-GP

LED-B-68-GF  
(83.0/1921.C70)

LED L

A

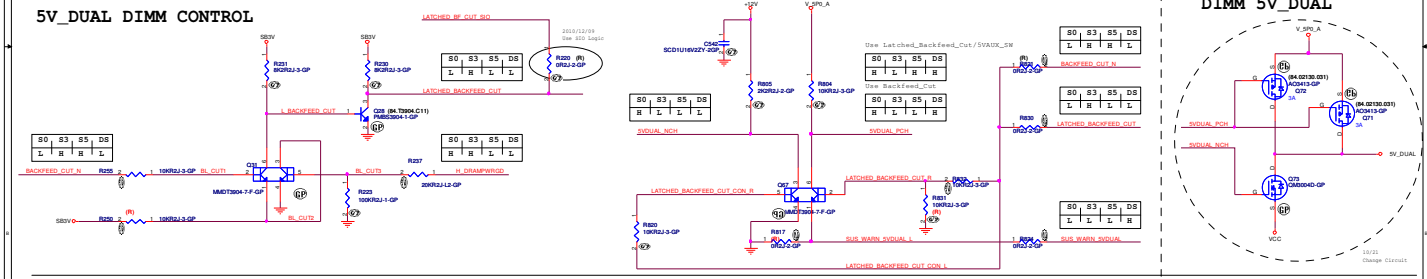
K

D29

<Variant Name>

**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

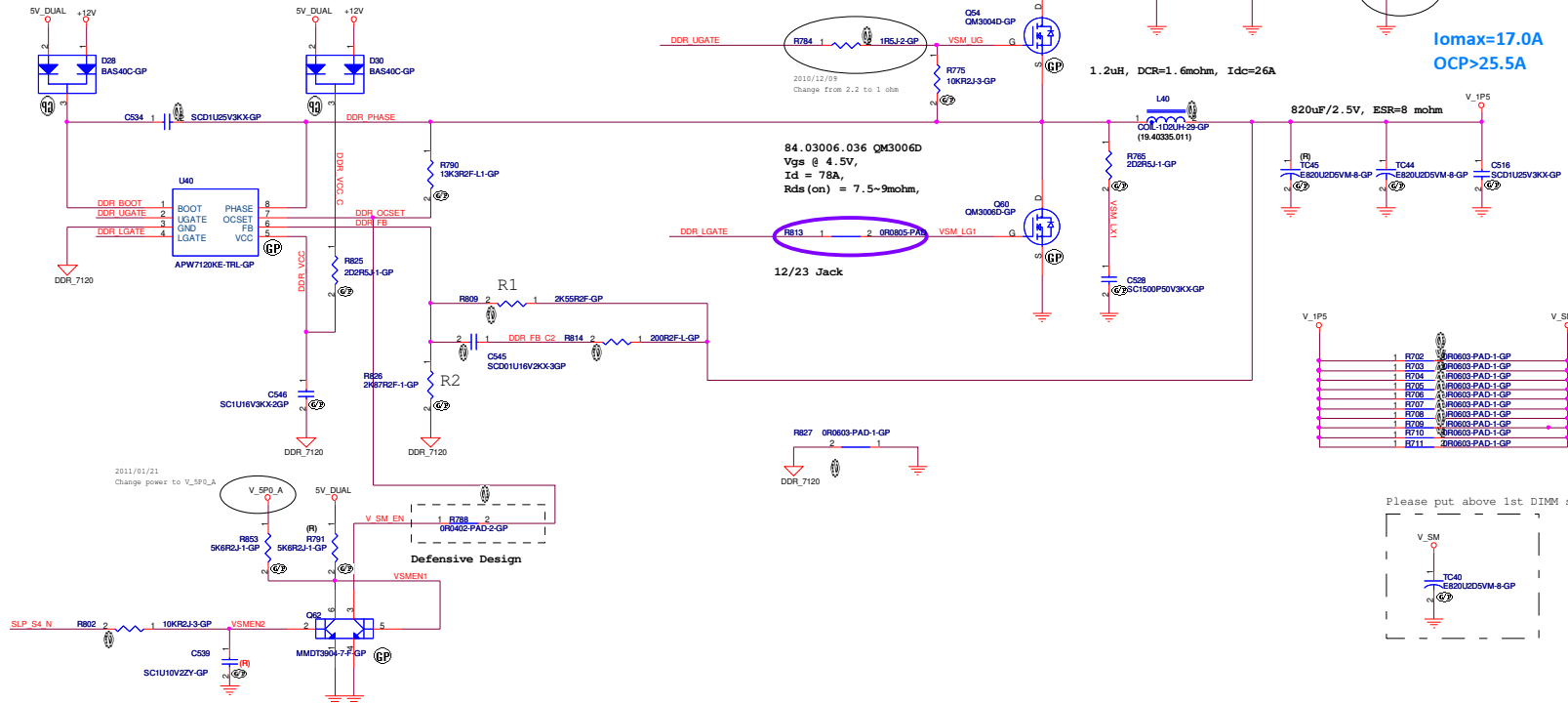
Title				
Size	Document Number			Rev
Custom	Rosa_Mission Hills			S
Date:	Sunday, March 20, 2011	Sheet	45	of 51

[illegible]

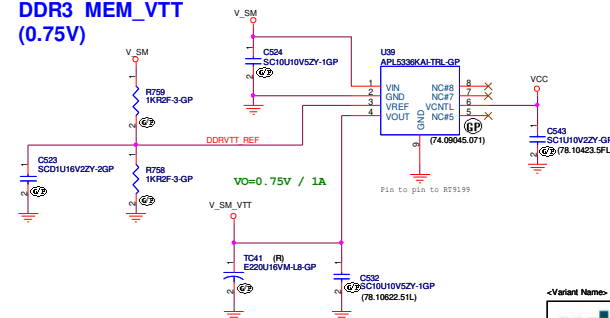
$$V_{out} = 0.8V(1+R1/R2)$$

$$I_{peak} = (40\mu A \cdot R_{ocset} - 0.4V) / R_{dson}$$

$$R_{ocset} = 13.3K, R_{dson} = 5.5m\Omega, I_{peak} = 24A$$



### DDR3 MEM\_VTT (0.75V)



<Variant Name>

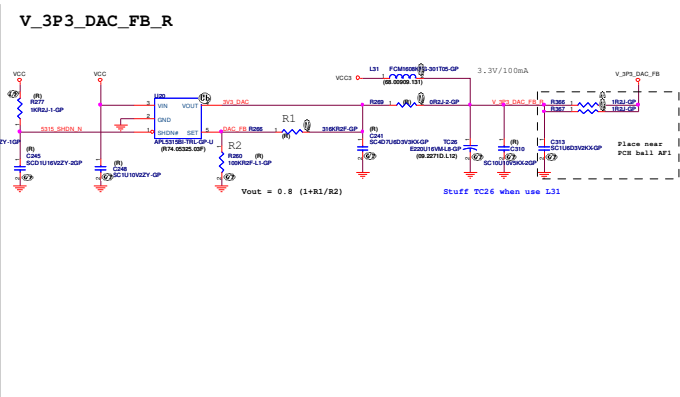
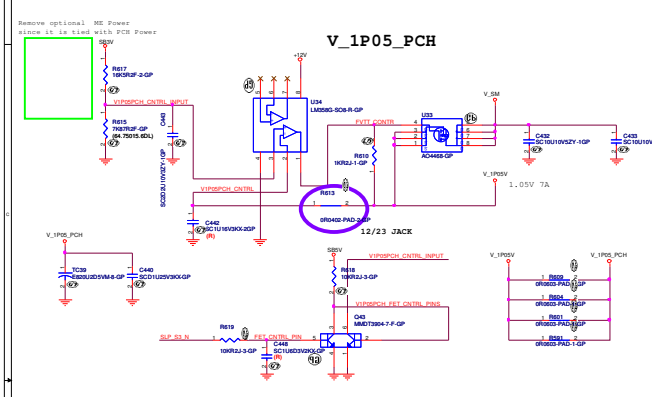
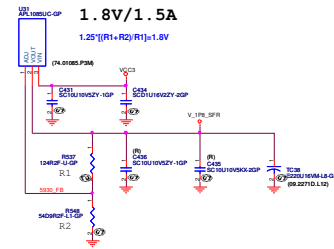
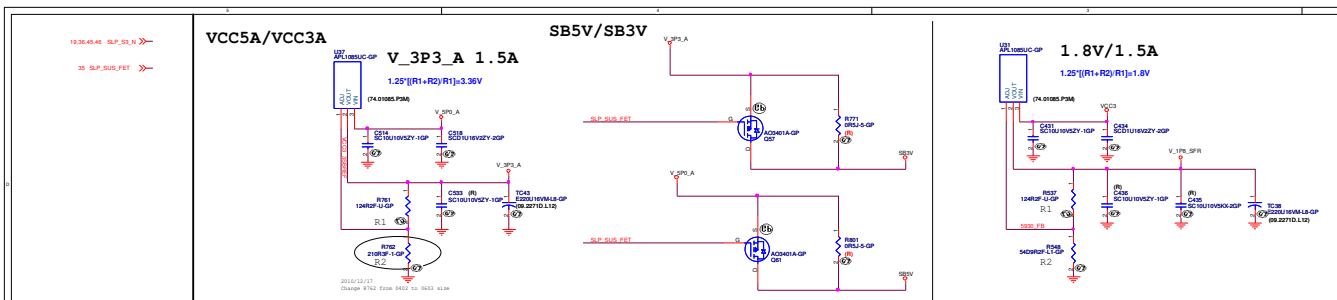
**wistron**

Wistron Incorporated  
21F, 88, Hein Tai Wu Rd  
Hsichih, Taipei

Title

Size C Document Number New SA

Date: Sunday, March 20, 2011 Sheet 47 of 51



Remove V\_1P05\_ME Circuit

Remove ME Defensive Circuit



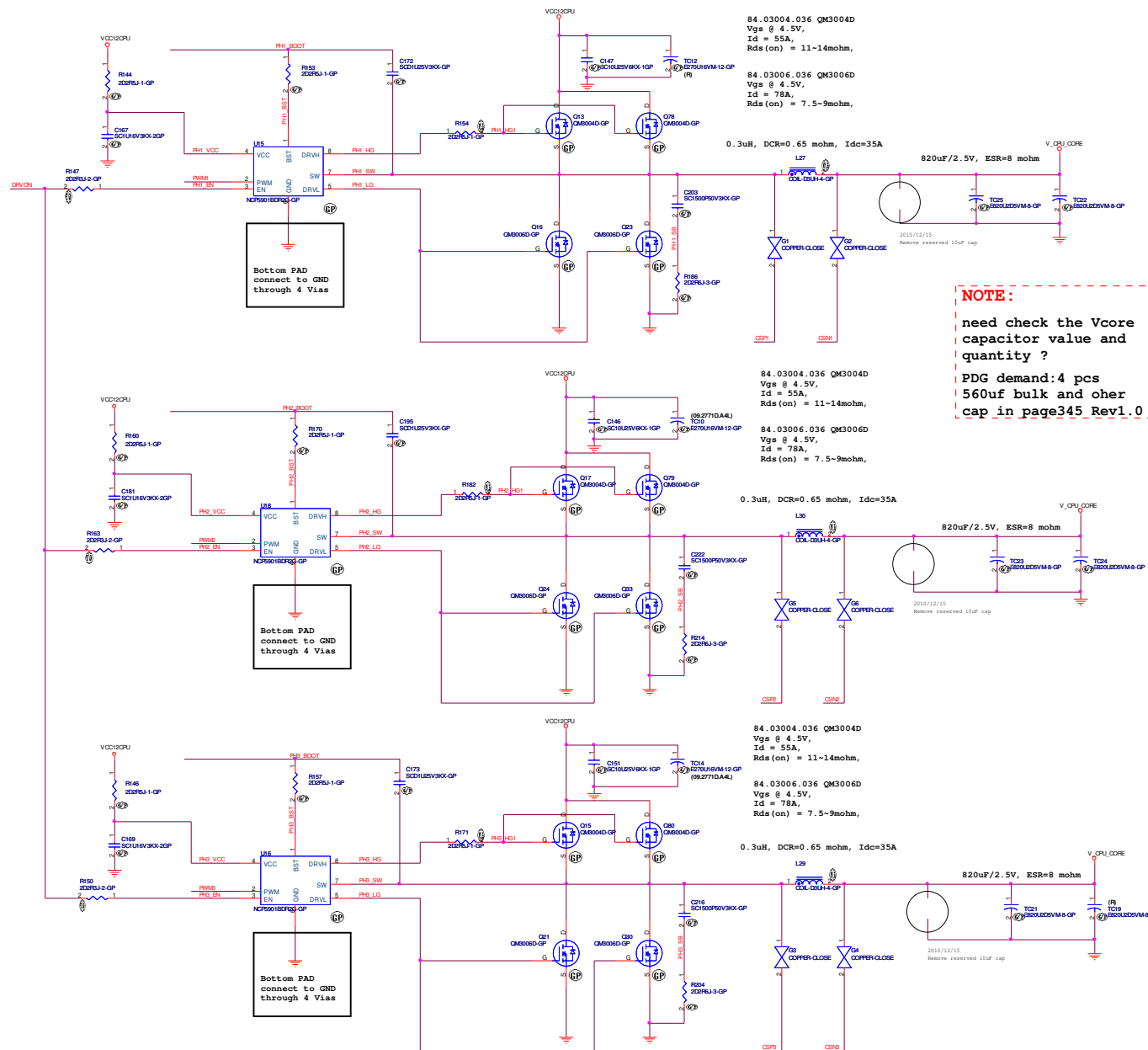




# CPU Vcore POWER

50 DRVON >>  
50 CPM1 >>  
50 CPM2 >>  
50 CPM3 >>  
50 CPM4 >>  
50 CPM5 >>  
50 CPM6 >>  
50 CPM7 >>  
50 CPM8 >>  
50 CPM9 >>  
50 CPM10 >>

## VCC\_CORE



-Variant Name-

<b>wistron</b>		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Heilsh, Taipei
File	Document Number	Rev
Custom	P000_M0000 H00	SA
Date	Sunday, March 20, 2011	Sheet 51 of 52